BRNO UNIVERSITY OF TECHNOLOGY
VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
DEPARTMENT OF MICROELECTRONICS

FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ
ÚSTAV MIKROELEKTRONIKY

INTEGRATED TEMPERATURE SENSOR BIPOLAR CORE

BACHELOR'S THESIS
BAKALÁŘSKÁ PRÁCE

AUTHOR JAKUB FRÁNEK
AUTOR PRÁCE

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NÁVRH BIPOLÁRNÍHO JÁDRA INTEGROVANÉHO TEPLOTNÍHO SENZORU

BACHELOR'S THESIS
BAKALÁŘSKÁ PRÁCE

AUTHOR — **Jakub Fránek**
AUTOR PRÁCE

SUPERVISOR — **Ing. Vilém Kledrowetz, Ph.D.**
VEDOUCÍ PRÁCE

BRNO 2018

BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

Bachelor's Thesis

Bachelor's study field **Microelectronics and Technology**
Department of Microelectronics

Student: Jakub Fránek ***ID:*** 186059

Year of study: 3 ***Academic year:*** 2017/18

TITLE OF THESIS:

Integrated temperature sensor bipolar core

INSTRUCTION:

Present the possible ways of implementing an integrated temperature sensor in contemporary CMOS process technologies and select a sensing method suitable for achieving high precision measurements within a wide temperature range. Utilising TSMC110 fabrication technology, design the sensor bipolar core and its biasing circuitry. Verify the functionality of the proposed circuits using Monte Carlo simulation across process and temperature variations and discuss the achieved results.

RECOMMENDED LITERATURE:

According to recommendations of supervisor

Date of project specification: 5.2.2018 ***Deadline for submission:*** 31.5.2018

Leader: Ing. Vilém Kledrowetz, Ph.D.
Consultant: Ing. Ivan Koudar, Ph.D., ON Design Czech s.r.o.

doc. Ing. Jiří Háze, Ph.D.
Subject Council chairman

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

Bakalářská práce

bakalářský studijní obor **Mikroelektronika a technologie**
Ústav mikroelektroniky

Student: Jakub Fránek ***ID:*** 186059
Ročník: 3 ***Akademický rok:*** 2017/18

NÁZEV TÉMATU:

Návrh bipolárního jádra integrovaného teplotního senzoru

POKYNY PRO VYPRACOVÁNÍ:

Představte možnosti realizace integrovaného teplotního senzoru v současných CMOS výrobních technologiích a vyberte koncepci umožňující dosažení vysoké přesnosti měření v širokém rozsahu teplot. Ve výrobní technologii TSMC110 navrhněte bipolární jádro senzoru a jeho napájecí obvody. Ověřte funkčnost navržených obvodů pomocí simulací Monte Carlo přes výrobní a teplotní rozptyl a vyhodnoťte dosažené výsledky.

DOPORUČENÁ LITERATURA:

Dle pokynů vedoucího

Termín zadání: 5.2.2018 ***Termín odevzdání:*** 31.5.2018

Vedoucí práce: Ing. Vilém Kledrowetz, Ph.D.
Konzultant: Ing. Ivan Koudar, Ph.D., ON Design Czech s.r.o.

doc. Ing. Jiří Háze, Ph.D.
předseda oborové rady

ABSTRACT

The aim of this thesis is to describe the main possible ways of implementing a smart temperature sensor on a silicon chip in common CMOS process technologies and to design an analog front-end of a bipolar transistor based smart temperature sensor in TSMC 110 process technology. Techniques such as chopping, dynamic element matching or trimming have been utilized to design circuits whose simulated 3σ measurement precision is $\pm 3.5\,^{\circ}\mathrm{C}$ untrimmed or $\pm 0.6\,^{\circ}\mathrm{C}$ after single point trim over the military temperature range. The designed circuits occupy as little as $0.012\,\mathrm{mm}^2$ of die area and their overall performance is comparable to the current state of the art.

KEYWORDS

temperature, sensor, CMOS, bipolar, TSMC 110, analog, IP core

ABSTRAKT

Cílem této práce je popsat možné způsoby realizace teplotního senzoru na křemíkovém čipu v běžných CMOS výrobních technologiích a představit konkrétní implementaci analogového jádra teplotního senzoru využívajícího bipolární tranzistory ve výrobní technologii TSMC 110. Techniky jako chopping, dynamic element matching nebo trimování byly použity k navržení obvodů, jejichž simulovaná 3σ přesnost měření je $\pm 3.5\,^{\circ}\mathrm{C}$ bez trimování nebo $\pm 0.6\,^{\circ}\mathrm{C}$ po jedné trimovací operaci napříč vojenským teplotním rozsahem. Navržené obvody zabírají pouze $0.012\,\mathrm{mm}^2$ plochy čipu a jejich celkové parametry jsou srovnatelné s výsledky současných publikovaných prací.

KLÍČOVÁ SLOVA

teplotní, senzor, CMOS, bipolární, TSMC 110, analogový, IP jádro

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DECLARATION

I declare that I have written the Bachelor's Thesis titled "Integrated temperature sensor bipolar core" independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the thesis and listed in the comprehensive bibliography at the end of the thesis.

As the author I furthermore declare that, with respect to the creation of this Bachelor's Thesis, I have not infringed any copyright or violated anyone's personal and/or ownership rights. In this context, I am fully aware of the consequences of breaking Regulation § 11 of the Copyright Act No. 121/2000 Coll. of the Czech Republic, as amended, and of any breach of rights related to intellectual property or introduced within amendments to relevant Acts such as the Intellectual Property Act or the Criminal Code, Act No. 40/2009 Coll., Section 2, Head VI, Part 4.

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INTRODUCTION

The need for integrated temperature sensors in commonly used Complementary Metal Oxide Semiconductor (CMOS) technologies can be explained by the fact that the performance of nearly all systems – not only electrical ones - depends upon their temperature. It is therefore desirable to enable silicon chips to measure their own temperature, as such information can be used for thermal management of high performance chips, for compensating unwanted temperature dependencies or simply for environmental temperature sensing.

Precision electronic temperature measurements have usually been done using discrete components such as platinum resistors or thermopiles, but these methods take up significant space on the circuit board, do not include the often necessary Analog to Digital Converter (ADC) and are significantly more expensive in high volume production than fully integrated solutions.

The so-called *smart temperature sensors* are integrated on chip and include an ADC of their own, which allows them to directly communicate with other digital circuits on the circuit board or even on the same silicon die. The latter is possible because these smart temperature sensors can be designed to take up small die area and are therefore often distributed as an Intellectual Property (IP) cores for use in customer Application Specific Integrated Circuits (ASIC). The advantages of smart temperature sensors were, however, often outweighed by their insufficient accuracy and lackluster performance at high temperatures. While it is possible to trim smart temperature sensors to achieve better than $\pm 1\,^{\circ}\mathrm{C}$ 4σ measurement inaccuracy over the industrial temperature range after two or more trimming operations, the logistical and temporal demands of such operations diminish the cost advantage of CMOS smart temperature sensors, which is what made them attractive in the first place. Both industrial and academic research has been therefore done to find ways to improve the accuracy of these sensors and lower the need for multiple trims using advanced circuit techniques such as Dynamic Element Matching (DEM), chopping, curvature compensating and others.

The chapter 1 of this thesis will present four basic methods that can be used to sense temperature on chip in contemporary CMOS processing technologies and compare them according to their advantages and disadvantages. The chapter 2 will describe the theoretical principles behind the bipolar transistor temperature sensing method in particular. The chapter 3 will present circuit solutions which can be used to implement this type of sensor and the associated errors of the circuits will be analyzed so that an error budget can be prepared. Finally, analog front-end of a bipolar transistor based smart temperature sensor in the TSMC 110 nm processing technology will be designed and its simulated performance presented in chapter 4.

1 SMART TEMPERATURE SENSORS

This chapter will provide an overview of conventional smart temperature sensor architecture and will present and compare four possible ways of sensing temperature in standard CMOS process technologies.

1.1 Smart temperature sensor architecture

Figure 1.1 depicts a simple block diagram of a smart temperature sensor. At the most basic level, the *analog front-end* (or *analog core*) consists of the sensing circuit and its biasing circuitry. The sensing circuit generates the analog signal carrying the temperature information, while the biasing circuits generate the DC voltages and currents the sensing circuit needs for its proper function.

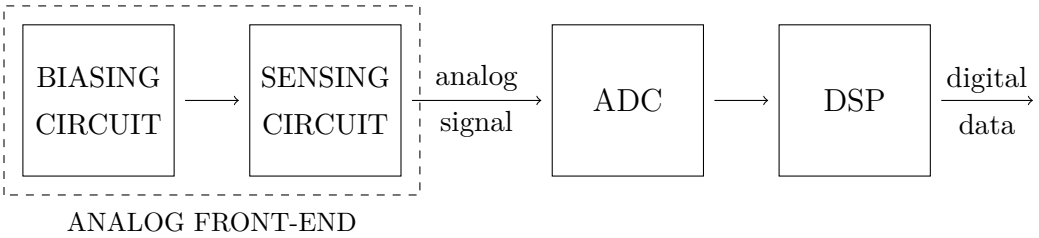


Fig. 1.1: Simple smart integrated temperature sensor block diagram

The other two blocks of smart temperature sensors are the ADC and Digital Signal Processing (DSP) circuits. The ADC converts the analog temperature information into a digital signal. Usually, temperature readings do not have to be taken at fast rates and frequencies of several readings a second are sufficient. This relaxes the sampling rate requirements on the ADC, which allows the designers to trade off speed for precision. This is the reason for why most precision smart temperature sensors utilize $\Sigma\Delta$ ADCs. These ADCs then require the DSP circuits to decimate the oversampled data, filter it with a digital low-pass filter and convert the data to a useful format.

1.2 Temperature sensing methods in standard CMOS process technologies

This section will present four possible ways of implementing the *sensing circuit* block from Figure 1.1 in standard CMOS process technologies. The sensing methods will be compared mostly according to the 3σ precision achieved in prior art.

It should be noted, however, that the cited implementations are academic in origin and their achieved precision was usually determined by measuring no more than 30 samples of chips, often originating from the same process batch. These designs would, if produced in high volumes over long period of time, eventually achieve significantly worse 3σ accuracy than the papers suggest.

1.2.1 Resistor method

The resistance of real resistors exhibits temperature dependence. In most analog circuits this dependence is inconvenient. It can be, however, used to sense die temperature. At the simplest level, it is possible to directly apply a reference voltage to the resistor and sense the current or vice versa in order to measure its resistance. The errors associated with this method are however very large. This is caused by the process spread, which heavily affects both the resistance value and the temperature coefficient of resistance (TCR) of the resistors. Non-linearity of the dependence is a significant source of error as well.

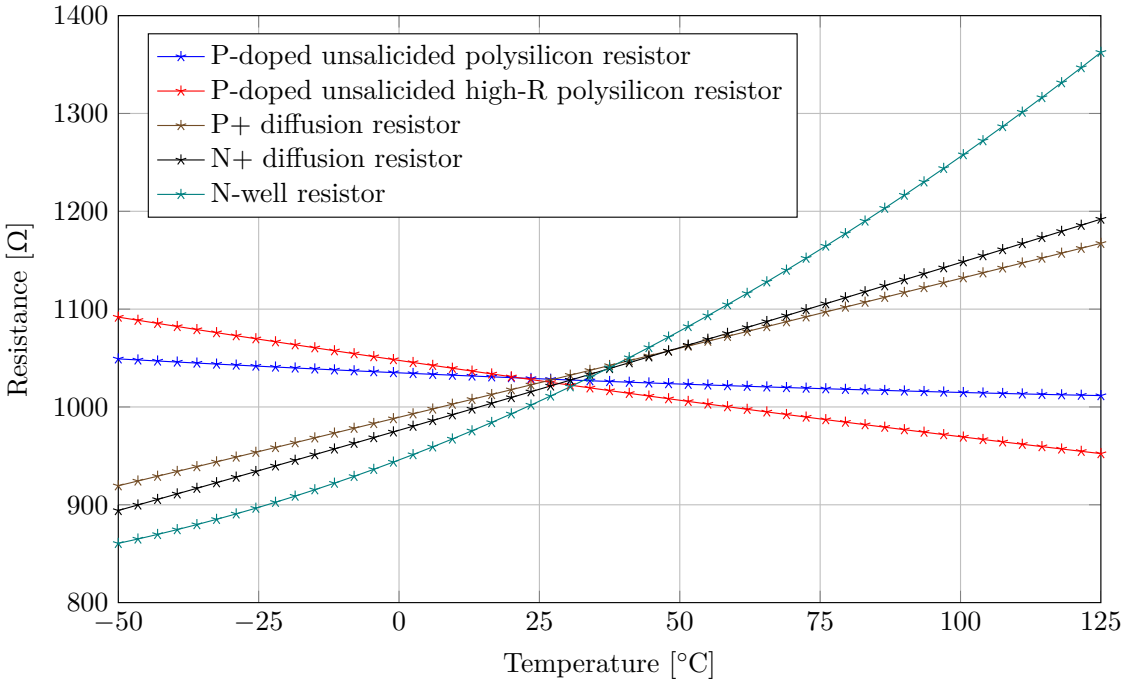


Fig. 1.2: Typical case resistance temperature dependence for selected resistor types in TSMC 110 process technology (nominal $R \approx 1\,\mathrm{k\Omega}$)

An alternative is to embed the resistors in a Frequency Locked Loop (FLL) and convert the temperature information into the frequency domain. Implementations such as [1] and [2] utilize this sensing method in order to compensate for the temperature dependence of Micro-Electro-Mechanical System (MEMS) silicon resonators

or external real time clock crystal oscillators respectively. These sensors are more immune to the above mentioned process variations, but they nevertheless require at least two costly trims to achieve accuracy better than $\pm 1\,^{\circ}\mathrm{C}$ at 3σ.

In summary, resistor based methods find their use in sensors meant either for crude measurements, for MEMS applications, or for extremely precise and stable sensors if multiple trimming operations are allowed, but other methods generally achieve better results while minimizing the financial costs [3, p.931].

1.2.2 Thermal diffusivity method

Thermal diffusivity based temperature sensors, also known as Electrothermal Filters (ETF), exploit the fact that the silicon that makes up the substrate is very pure and only lightly doped, as the concentration of dopant atoms in the substrate is on the order of few ppm relative to concentration of pure silicon [4, p.68]. Consequently, the thermal diffusivity (D) of silicon is relatively insensitive to doping fluctuations and follows a predictable temperature dependence $D \propto T^{1.8}$ [5].

The implementation of these sensors consists of a heater element (a resistor) surrounded by temperature sensing elements (often thermopiles made from resistors and aluminum interconnects). The operating principle is depicted on Figure 1.3. Constant frequency current pulses are passed through the heater resistor, dissipating power into the silicon and producing temperature fluctuations which propagate through the silicon and which are sensed by the surrounding thermopiles. The delay

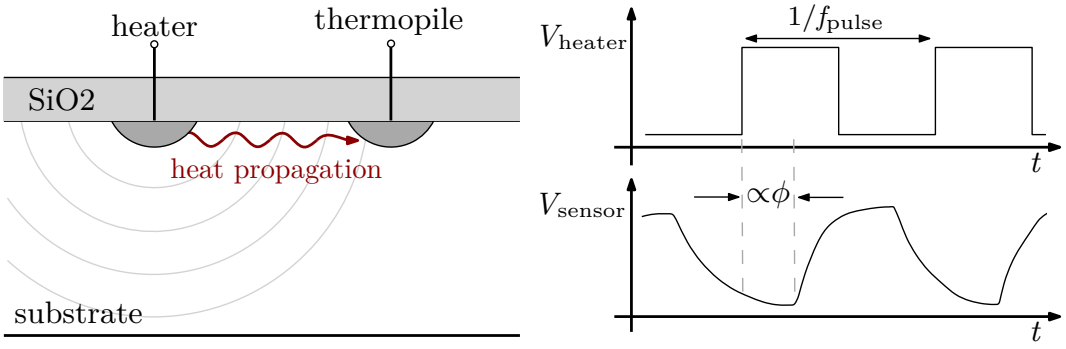


Fig. 1.3: Thermal diffusivity based temperature sensors operating principle

or phase shift between the sensed temperature fluctuations and the original pulses is related to D. Because D is dependent on temperature, this phase shift can be used to determine the junction temperature of the chip. In that sense, the sensing circuit serves as a temperature to phase shift converter.

While the resistors used in the sensor are subject to the same errors and non-linearities described in subsection 1.2.1, this method is not affected by them, because

it is the phase shift and not the resistance which is measured. This can lead to accurate measurements over extremely wide temperature range without any trimming necessary, as demonstrated in [4], where $\pm 0.6\,^{\circ}\mathrm{C}$ untrimmed accuracy was achieved from $-70\,^{\circ}\mathrm{C}$ up to $225\,^{\circ}\mathrm{C}$. ETF sensors can also be implemented in advanced process nodes such as 40 nm while still achieving above average precision with single point trim ($\pm 1\,^{\circ}\mathrm{C}$) on die areas as small as $1650\,\mu\mathrm{m}^2$, as documented in [6]. This is especially attractive for System on Chip (SoC) applications.

On the other hand, it is difficult to simulate and verify this sensor architecture during the design process as no circuit simulator is capable of modeling the propagation of heat through the substrate, let alone the function of the thermopiles. Another disadvantage is that comparatively large power consumption (on the order of several mW) is unavoidable in order to generate measurable thermoelectric voltages, which precludes them from use in battery or Radio Frequency Identification (RFID) chip applications. Even then low noise and very slow (< 1 S/s) high precision $\Sigma\Delta$ ADCs are necessary because the voltages generated by the thermopiles are on the order of tens of microvolts [4, p.68]. At this level, the thermal noise of all the components that make up the smart sensor is a significant source of error which needs to be filtered out over time by the ADC, thus lowering the frequency of measurements. Finally, the untrimmed precision of [4] is only possible for circuits manufactured on expensive Silicon on Insulator (SOI) wafers. The extra insulating layer can limit the thermal losses to substrate, which do not produce any useful signal in the thermopiles, and therefore improve both the signal-to-noise ratio (SNR) and the power efficiency of the sensor [4, p.66]. The SOI technology, however, brings its own set of issues, such as increased self-heating and less effective cooling [7], which makes it unattractive for high power analog or high performance digital applications, which are applications that would benefit from integrating a wide temperature range smart temperature sensors in the first place.

These disadvantages can be outweighed by the advantages for some ASICs, but along with the high design difficulty and risk, they limit the usefulness of this type of sensor in many common applications.

1.2.3 Bipolar transistor method

The Bipolar Junction Transistor (BJT) is the most common sensing element in smart temperature sensors fabricated in analog-compatible CMOS processes [3, p.931]. The reason for this is identical to the reason for why band gap voltage references are so common: the process dependence of bipolar transistor I-V characteristics is small compared to the alternatives.

In most cases, the sensing circuit features at least two diode-connected BJTs

(whose collector and base are tied together) which are biased at different current densities (i.e. either the emitter areas or the bias currents differ). The base-emitter voltage (V_{BE}) developed across the transistors is Complementary To Absolute Temperature (CTAT) while the difference between the V_{BE} voltages ΔV_{BE} is Proportional To Absolute Temperature (PTAT). Because these voltages are approximately linear functions of temperature, a linear combination of these voltages can produce a voltage independent of temperature, usually called V_{REF}, which is approximately equal to the band gap voltage of silicon for T=0 K (V_{g0}). Band gap voltage references produce this voltage as accurately as possible. This is illustrated on Figure 1.4.

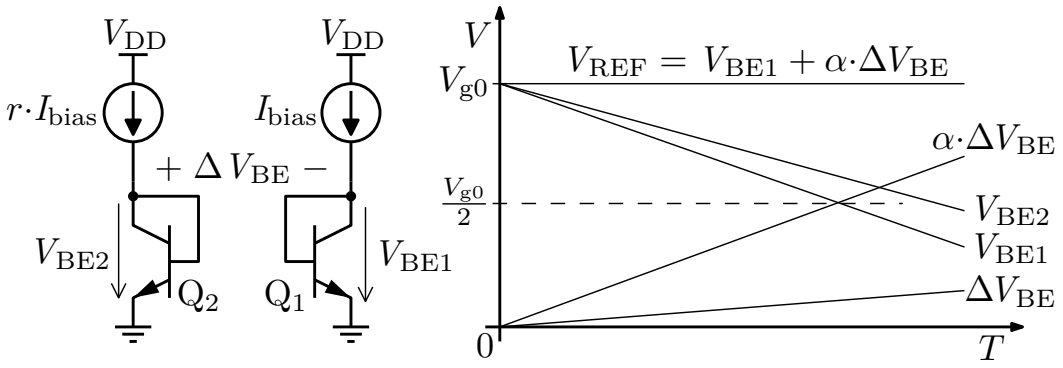


Fig. 1.4: Band gap voltage reference operating principle

As smart temperature sensors need to produce a signal that is strongly PTAT or CTAT in order to represent the analog temperature information, producing the reference voltage is theoretically not necessary. However, because the temperature dependent signal needs to be measured against a reference in the ADC so that the temperature can be correctly evaluated in the digital domain, BJT-based smart temperature sensors produce the band gap reference voltage anyway.

The V_{BE} voltage can be modeled by the following equation

$$V_{\mathrm{BE}} = \frac{kT}{q} \cdot \ln \frac{I_{\mathrm{C}}}{I_{\mathrm{S}}(T)} \tag{1.1}$$

where k is the Boltzmann constant, T is thermodynamic temperature, q is the elementary charge, I_{C} is the collector current and I_{S} is the saturation current. The expression $\frac{kT}{q}$ is also known as the thermal voltage V_{T}. The saturation current is a quantity which includes the process dependent parameters of the device and it is the primary source of error in the circuit. The saturation current is also heavily temperature dependent and causes the typical V_{BE} slope of approximately $-2\,\mathrm{mV\,K^{-1}}$.

An interesting property of ΔV_{BE} is that it does not depend on I_{S} and is therefore process independent. This will be derived and discussed in greater detail in subsection 2.1.1. The immunity to process variation makes ΔV_{BE} an ideal signal to digitize

in the ADC and derive the die temperature from. However, because the smart temperature sensor needs a reference voltage and the reference voltage is a product of V_{BE}, I_{S} inevitably affects the measurement error indirectly (unless external reference voltage source is used, which is not common in IP core implementations).

While the BJT-based temperature sensors cannot reach the untrimmed accuracy of ETF-based sensors, they are verified more easily using conventional circuit simulators and do not require expensive process options such as SOI. While CMOS processes are optimized for Metal Oxide Semiconductor (MOS) transistors, some types of BJT devices are available in all CMOS processes which preserves the cost advantage of smart temperature sensors. BJT-based sensors can also offer power consumption on the order of few µW, attractive for battery or RFID tag applications. Finally, a substantial advantage of BJT-based sensors is the large amount of literature and research available on the topic, which makes the design process less time consuming and risky.

Some of the most successful recent implementations of BJT-based temperature sensors are shown in [8] and [9]. The former implementation combined batch calibration with single room-temperature trim and achieved $\pm 0.25\,^{\circ}\mathrm{C}$ accuracy from $-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ (160 nm process). The latter sensors' accuracy is $\pm 0.3\,^{\circ}\mathrm{C}$ from $-45\,^{\circ}\mathrm{C}$ to $130\,^{\circ}\mathrm{C}$ (0.7 µm process) with only one single-point trim.

1.2.4 MOS transistor method

Using a MOS transistor as the sensing element would be highly desirable because in CMOS processes, MOS transistors are the best optimized, the best characterized and also the most area efficient devices available to designers. Some smart temperature sensor implementations utilizing MOS transistors are purely digital and do not even include a conventional ADC, which is especially advantageous for modern digital oriented process nodes.

Examples of the purely digital smart temperature sensors include inverter delay or ring oscillator based sensors. Both of these methods convert the temperature information into time domain via inverter gate propagation delay, which is dependent on two temperature dependent quantities, namely threshold voltage (V_{th}) and charge carrier mobility (μ) [10, p.11]. This direct temperature to time conversion allows these sensors to circumvent the need for an ADC as the time information can be processed using standard digital elements such as counters or phase detectors. These sensors are often called *time-to-digital* or *all-digital time-domain* sensors. Accuracies of $\pm 1\,^{\circ}\mathrm{C}$ have been reported in [11] and [12], both of these implementations however relied on expensive two point trim after packaging and their operating range itself was only $0 - 100\,^{\circ}\mathrm{C}$. As prior art such as [13] and [14] documents, it is possible to

perform only a single point trim, but the errors are as large as ±3 °C. Finally, a notable implementation of the time-to-digital architecture is shown in [15], where the design was implemented on commercially available Field Programmable Gate Array (FPGA) and achieved single point trim accuracy of ±2.5 °C.

The other possibility is to use a diode-connected MOS transistor similarly to bipolar band gap circuits, where two MOS transistors biased at different current densities are used to generate CTAT signal V_{GS} and a PTAT signal ΔV_{GS}. This is possible only in the subthreshold region, defined by $V_{\mathrm{GS}} < V_{\mathrm{th}}$. Also known as the weak inversion region, this region of operation is an exception to the quadratic relationships that model the I-V characteristics of MOS transistors in the strong inversion region. In subthreshold operation, the gate-source voltage (V_{GS}) of a diode-connected MOS transistor behaves according to the equation

$$V_{\mathrm{GS}} = V_{\mathrm{th}}(T) + \frac{\eta k T}{q} \cdot \ln \frac{I_{\mathrm{D}}}{I_0(T)} \tag{1.2}$$

where η is the subthreshold slope factor and I_0 is a process and temperature dependent parameter [3]. The similarity with the equation (1.1) is obvious (I_0 being the MOS equivalent of I_{S}), there are, however, some important differences, the most important one being the fact that V_{th} is both process and temperature dependent. The MOS transistor is therefore significantly more sensitive to process variation and as a sensing element cannot reach the performance of BJTs.

MOS transistor based sensors may, however, be the best solution available for low voltage applications. Because the band gap voltage of silicon is approximately 1.25 V, the minimum supply voltage for circuits which include it is around 1.5 V (at least one $V_{\mathrm{DS\,sat}}$ above the band gap voltage). The threshold voltage V_{th} is significantly lower than that, and can be made even lower by connecting the MOS transistor in a Dynamic Threshold MOS (DTMOS) configuration. This is done by connecting the gate and the bulk, which in common n-well based CMOS processes is possible for PMOS transistors without any additional cost. This connection makes V_{th} dynamic and thus better defined, which decreases the process spread sensitivity of the sensor. Because increasing V_{GS} in DTMOS configuration further decreases V_{th}, the DTMOS transistor requires even less V_{GS} voltage to turn on. According to [16], supply voltages lower than 1 V are possible. A disadvantage of DTMOS transistors is the increased leakage current, and the potential for latch-up and possible subsequent destruction of the device – the V_{GS} voltage should not be able to surpass the turn-on voltage of the parasitic PNP transistor embedded inside the structure of the device (depicted on Figure 1.5).

One of the first implementations of a DTMOS-based temperature sensor is documented in [16]. The design achieved batch-calibrated accuracy of ±1.5 °C, which was

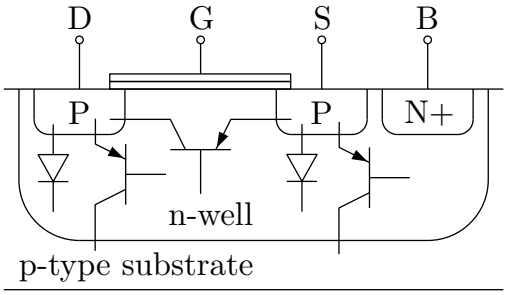


Fig. 1.5: N-well process PMOS cross-section with parasitic devices shown

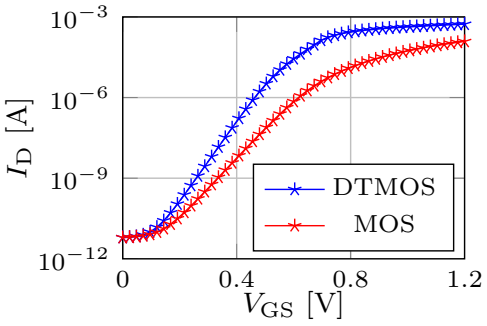


Fig. 1.6: MOS and DTMOS comparison

further improved after single point trim to ±0.4 °C over the military temperature range of −50 °C to 125 °C, which nearly rivals the precision of BJT-based sensors.

1.2.5 Summary of temperature sensing methods

Which of the previously discussed sensing methods is the best is always dependent on the particular application and its specifications. In general, their difference can be summarized as follows.

The resistor method is very crude and requires two or more trims to reach reasonable precision, but it is well suited for MEMS applications, and if the economical disadvantage of the numerous trimming operations is not an issue, resistor based sensors can be very precise, stable and simple to design.

Thermal diffusivity based sensors are extremely precise over wide temperature range and take up small area, but they consume a lot of power and they are difficult to simulate and verify, which makes them quite risky and therefore this technique has not been adopted by the industry yet.

Temperature sensing utilizing MOS transistors is the method of choice for low voltage applications or when fully digital approach has to be taken, but otherwise they offer no significant advantage compared to the alternatives as their processing spread is significant.

Finally, BJT-based temperature sensors are the most popular because they do not posses any significant disadvantage. Other methods may be better at some specific aspects which have been mentioned above, but BJT-based temperature sensing is usually the method of choice for general applications as it achieves decent performance in nearly every area with only one point trim. The fact that this method is well researched and documented in available literature is a benefit as well as the design is more straightforward and the risk is low.

2 THEORY OF BIPOLAR TRANSISTOR BASED SMART TEMPERATURE SENSORS

This chapter will focus solely on the BJT-based smart temperature sensors' theory of operation and architecture. It will discuss the device characteristics of bipolar transistor in contemporary CMOS technologies, provide a system level overview of the BJT-based smart sensor architecture and categorize the errors in the analog front-end of the sensor. The findings from this chapter will be later used in chapter 3, where the analog front-end circuits will be described in greater detail at the transistor level and thoroughly analyzed.

2.1 Bipolar transistor characteristics

The following subsections will discuss the basic BJT physics equations and technological characteristics.

It should be noted that this thesis will, in accordance with literature, use the technically incorrect convention for voltage direction across the PNP transistor. For forward biased PNP transistors there is a positive V_{EB} voltage developed from the emitter to the base. Literature on band gap references etc. has, however, adopted using V_{BE} interchangeably for both PNP and NPN transistors, therefore V_{BE} in the case of PNP transistors should be understood as $|V_{\mathrm{BE}}|$.

2.1.1 I-V characteristics

The commonly known equation modeling the relationship between V_{BE} and I_{C} is

$$I_{\mathrm{C}} = I_{\mathrm{S}} \cdot \exp \frac{qV_{\mathrm{BE}}}{kT} \tag{2.1}$$

After rearranging, this equation leads to (1.1). The equation (2.1) is, however, not accurate for diode-connected devices, as some assumptions "hidden" in the above equation concerning the carrier concentrations at the base-collector junction are no longer true. A better model is the following equation [17, p.17]:

$$I_{\mathrm{C}} = I_{\mathrm{S}} \cdot \left(\exp\left(\frac{qV_{\mathrm{BE}}}{kT}\right) - 1 \right) \tag{2.2}$$

The V_{BE} equation given by rearranging (2.2) is therefore changed to

$$V_{\mathrm{BE}} = \frac{kT}{q} \ln \frac{I_{\mathrm{C}} + I_{\mathrm{S}}}{I_{\mathrm{S}}} \tag{2.3}$$

The PTAT quantity ΔV_{BE} can be derived as follows

$$\begin{aligned}\Delta V_{\mathrm{BE}} &= \frac{kT}{q}\ln\frac{r\cdot I_{\mathrm{C}}+I_{\mathrm{S}}}{I_{\mathrm{S}}}-\frac{kT}{q}\ln\frac{I_{\mathrm{C}}+I_{\mathrm{S}}}{I_{\mathrm{S}}}= \\ &= \frac{kT}{q}\ln\left(\frac{r\cdot I_{\mathrm{C}}+I_{\mathrm{S}}}{I_{\mathrm{S}}}\cdot\frac{I_{\mathrm{S}}}{I_{\mathrm{C}}+I_{\mathrm{S}}}\right)= \\ &= \frac{kT}{q}\ln\frac{r\cdot I_{\mathrm{C}}+I_{\mathrm{S}}}{I_{\mathrm{C}}+I_{\mathrm{S}}}\end{aligned} \tag{2.4}$$

where r is the ratio between the current densities passing through the devices. The implication of (2.4) is that as long as I_{C} is much greater than I_{S}, ΔV_{BE} is approximately

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q}\ln r \tag{2.5}$$

This finding is important as it means that ΔV_{BE} can be made immune to changes in I_{S} and therefore nearly perfectly process independent simply by choosing a large enough value of biasing current. The value of I_{S} rises rapidly with temperature, but it usually does not exceed values of 10^{-12} A even at the top of the military temperature range – it is therefore easy to diminish its effect on ΔV_{BE}.

The collector current should not be, however, chosen arbitrarily high for three reasons. The obvious one is increased power consumption and the associated self-heating, which requires no further commentary. The second one is the effect of series resistance which is intrinsic to the transistor and which manifests as a voltage error directly adding to the values of V_{BE} or ΔV_{BE} – the larger the biasing current, the larger the error. Finally, when the collector current is high enough, (2.2) is no longer true either – the transistor enters the high-injection region of operation (the minority charge carrier density in base is no longer much smaller than the doping density) and the transistors' current gain β will begin to drop considerably.

It is therefore important to find a range of currents large enough to diminish the effect of I_{S} but simultaneously low enough to retain high β, low power consumption and low series resistance induced voltage error. The range changes considerably between process technologies and BJT device types and areas, and it is not guaranteed that this range exists in the first place. The optimum range of currents is the range where β is at its maximum value and current independent in all Process-Voltage-Temperature (PVT) conditions. In the case of TSMC 110 process technology, currents from approximately 1 nA to about 100 µA are ideal for biasing. This can be seen on Figure 2.1 which shows the dependence of β on I_{E}, temperature (depicted by color) and process spread (process corners depicted by markers).

It is important to note that the shape of the curves generated by the TSMC 110 model files does not align with the models of other similar and better characterized process nodes available to the author, which usually follow the shape of the green

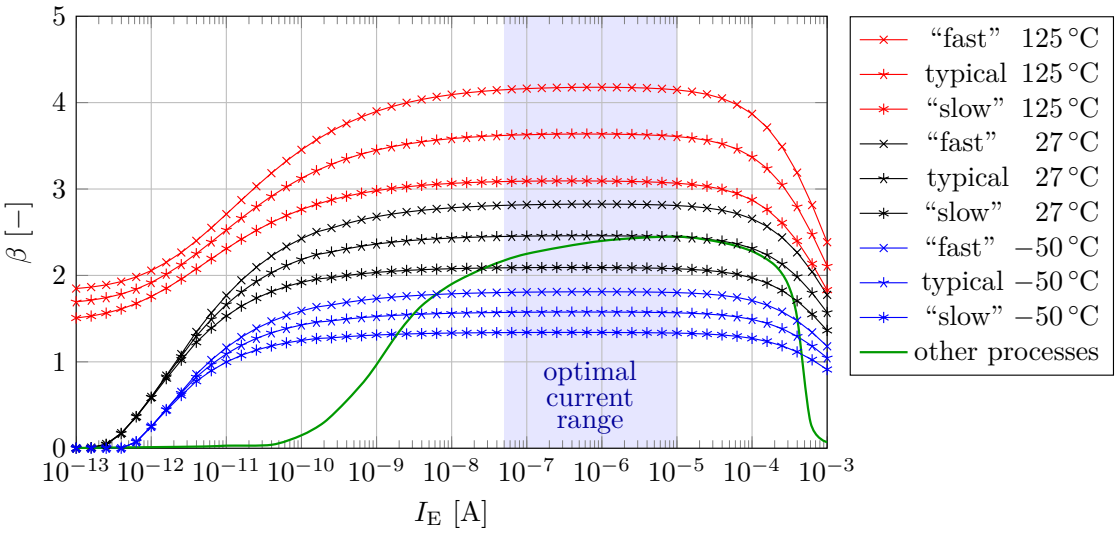


Fig. 2.1: Emitter current, temperature and process dependence of β of the *vpnp5* device in TSMC 110 process technology with the optimum current range highlighted

line on Figure 2.1. It is unrealistic to expect that β is current independent on current range this wide as suggested by the TSMC 110 models. The model files of TSMC 110 are probably untrustworthy in this respect and it is better to take the other similar process technologies into account when determining the ideal current range. Currents ranging from 50 nA to about 10 µA should be a safe choice as far as β goes, though the series resistance and the saturation current should also be kept in mind when deciding the actual value of the biasing current. This range is highlighted by a blue rectangle on Figure 2.1. It is slightly positioned towards the lower currents because there is an uncertainty associated with the green curve and its safer to err on the side where β does not drop off as steeply.

2.1.2 Saturation current and the curvature of V_{BE}

The saturation current of a PNP transistor is given by the following equation [18, p.380]

$$I_S = \frac{q\, D_p\, A_E\, n_i^2}{W_B\, N_D} = \frac{k\, T\, \overline{\mu_p}\, A_E\, n_i^2}{W_B\, N_D} \tag{2.6}$$

where A_E is the emitter area, n_i is the intrinsic carrier concentration, D_p is the hole diffusion constant, $\overline{\mu_p}$ is the effective hole mobility, W_B is the width of the base region and N_D is the concentration of donors in the base region. The concentration of donors in the base region N_D is obviously dependent on Random Dopant Fluctuation (RDF), while A_E and W_B can be subject to lithographic errors and diffusion depth spread. The intrinsic carrier concentration n_i and the effective hole mobility $\overline{\mu_p}$

should be precise under normal conditions, but they can be altered by mechanical stress applied to the chip during packaging [19].

The random spread of saturation current manifests itself as an error in V_{BE} which increases with temperature (also known as PTAT error). This can be proved as follows

$$\begin{aligned} V_{\mathrm{BE}} &= \frac{kT}{q}\ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}+\varepsilon(I_{\mathrm{S}})}\right) = \frac{kT}{q}\ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}+\varepsilon(I_{\mathrm{S}})}\cdot\frac{1/I_{\mathrm{S}}}{1/I_{\mathrm{S}}}\right) = \\ &= \frac{kT}{q}\ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right) - \frac{kT}{q}\ln\left(\frac{I_{\mathrm{S}}+\varepsilon(I_{\mathrm{S}})}{I_{\mathrm{S}}}\right) = V_{\mathrm{BE}}|_{\varepsilon(I_{\mathrm{S}})=0} - \frac{kT}{q}\ln\left(\frac{I_{\mathrm{S}}+\varepsilon(I_{\mathrm{S}})}{I_{\mathrm{S}}}\right) \approx \\ &\approx V_{\mathrm{BE}}|_{\varepsilon(I_{\mathrm{S}})=0} - \frac{kT}{q}\cdot\frac{\varepsilon(I_{\mathrm{S}})}{I_{\mathrm{S}}} = V_{\mathrm{BE}}|_{\varepsilon(I_{\mathrm{S}})=0} - \frac{kT}{q}\cdot\delta(I_{\mathrm{S}}) \end{aligned} \tag{2.7}$$

where $\varepsilon(I_{\mathrm{S}})$ is the absolute error or deviation associated with I_{S}, $\delta(I_{\mathrm{S}})$ is its relative error and where the approximation $\ln(1+x) = x$ for $x \ll 1$ was used. The error term in the equation above increases linearly with temperature, the random spread of V_{BE} is therefore PTAT, as evidenced by Figure 2.2.

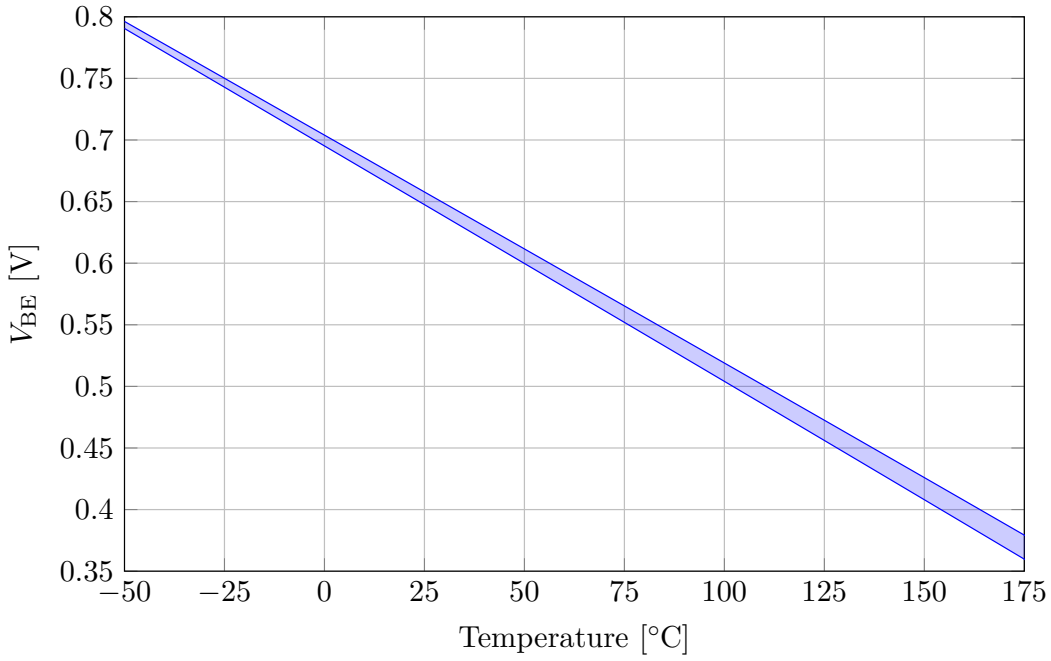


Fig. 2.2: Process spread of V_{BE} of a substrate PNP BJT in TSMC 110

The saturation current is not only process dependent, which is a significant source of random error, it is also temperature dependent, which gives rise to the curvature of V_{BE}. This is, in turn, a source of systematic non-linearity of the measurement. The mathematical origin of the curvature will be derived below.

The temperature dependence of I_S can be written as follows [17, p.21]

$$I_S = CT^{\eta} \exp\left(\frac{-qV_{g0}}{kT}\right) \tag{2.8}$$

where C is a constant and η is a parameter usually ranging from 3 to 4 in most processes. This equation is also implemented in SPICE – the SPICE model parameters `EG` and `XTI` are equivalent to V_{g0} and η respectively. For TSMC 110 substrate bipolar transistor, `EG` = 1.16 V and `XTI` = 3. Combining with (1.1) reveals why V_{BE} approaches V_{g0} for $T \to 0\,\mathrm{K}$:

$$\begin{aligned} V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{CT^{\eta} \exp(\frac{-qV_{g0}}{kT})}\right) = \frac{kT}{q}\left[\ln\left(\frac{I_C}{CT^{\eta}}\right) + \ln\left(\exp\left(\frac{qV_{g0}}{kT}\right)\right)\right] = \\ = V_{g0} + \frac{kT}{q} \ln\left(\frac{I_C}{CT^{\eta}}\right) \end{aligned} \tag{2.9}$$

The reason for why V_{BE} falls with rising temperature is that the logarithm evaluates to a negative number. This is because the expression inside the logarithm is smaller than one, as the collector current is usually in the order of nano to micro Amperes and the temperature in Kelvin to the power of 3 is around 10^7 to 10^8 K. The value of C is difficult to find out exactly – for the transistors in TSMC 110, values of around 0.0001 seems to fit the simulated behavior. This makes the expression inside the logarithm evaluate to around $37 \cdot 10^{-12}$, which makes the logarithm as a whole evaluate to approximately -24. The product of $-24 \cdot \frac{k}{q}$ is around $-2.07\,\mathrm{mV\,K^{-1}}$, which is in the range of the usual slopes of V_{BE}.

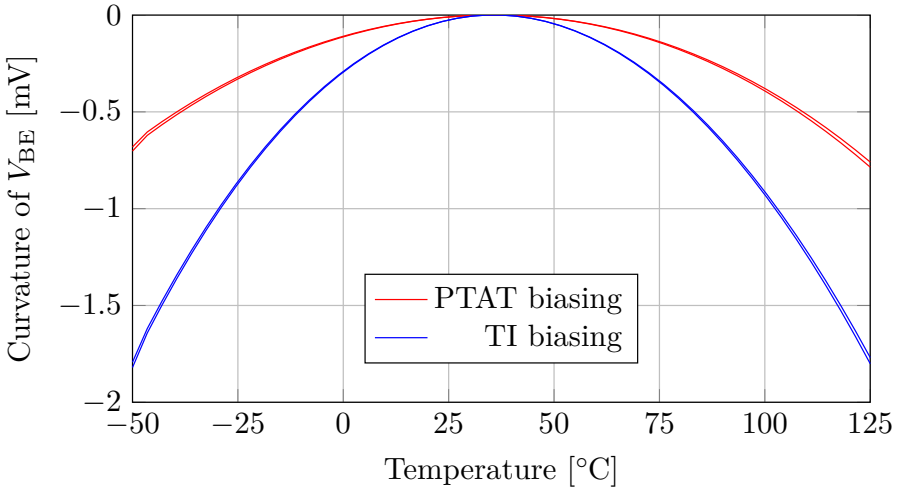


Fig. 2.3: Curvature of V_{BE} of a substrate PNP BJT in TSMC 110 for TI and PTAT biasing current including its spread

If the logarithm term were to be temperature independent, V_{BE} would be a perfect line, as its slope would be constant over the whole temperature range. However,

because there is a temperature term in the denominator of the expression inside the logarithm, the slope of V_{BE} is temperature dependent as well, and it becomes more negative the higher the temperature. This makes V_{BE} follow a concave line with regards to temperature as seen on Figure 2.3 for temperature independent current biasing. The graph shows the process spread of the curvature as well, which is negligible. This non-linearity is undesirable, as it makes the sum of $V_{\mathrm{BE}} + \alpha \cdot \Delta V_{\mathrm{BE}}$ curved as well. Curvature compensation is therefore required.

This section will not describe all the possible ways of reducing the curvature of V_{BE}, but one simple method can be mathematically deduced from (2.9). If the collector current were to be temperature dependent the same way as the term T^{η}, these terms would cancel out. Implementing a T^{η} current source is difficult, as η is around 3 to 4, but utilizing a PTAT current source (T^1) is simple and at least some curvature can be eliminated this way, as Figure 2.3 shows. This biasing technique is doubly beneficial, because not only it decreases curvature, PTAT current can be made comparatively less process dependent, because it can be derived from the process independent PTAT signal ΔV_{BE}.

Another curvature compensation method will be shown later in subsection 3.3.3.

2.1.3 Bipolar devices in CMOS process technologies

Most low cost CMOS process technologies are n-well based, which means that they use a P-type substrate. There are many reasons for this, such as the fact that most ICs are designed to use common ground rather than common positive supply voltage rail, or because it is desirable to use NMOS devices rather than PMOS ones whenever possible because of their better performance for given size. In these technologies, it is possible to manufacture two types of BJT devices without any costly additional technological steps: the lateral PNP and the vertical PNP transistors.

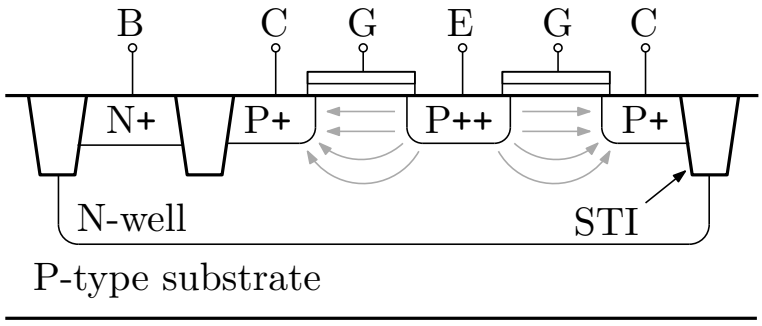


Fig. 2.4: Cross-section of typical lateral BJT device in CMOS process technologies

Lateral PNP transistors are based on PMOS transistors where the bulk serves as the base and the gate is connected to positive voltage so that it does not affect the

transistors performance. Their β is relatively large, but they suffer from a parasitic PNP embedded in their structure which causes a significant current flow from the emitter to the substrate. Their $I_C - V_{BE}$ characteristic is highly non-ideal as well because of current crowding effects as shown on Figure 2.4 – when the current density is high, the additional emitter current has to take a longer curved trajectory to the collector. Many of their parameters are therefore current dependent which is highly undesirable for precision design.

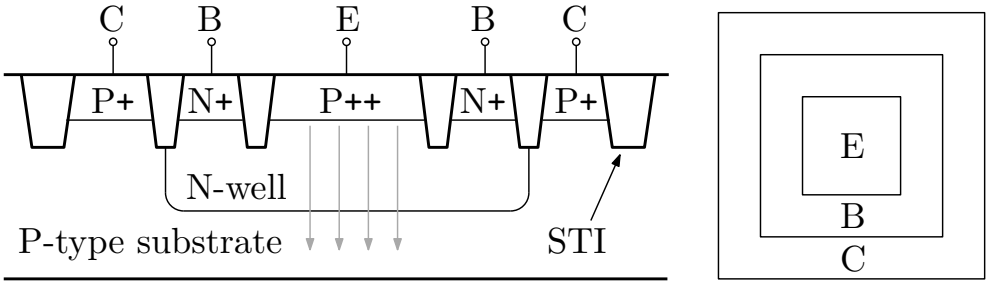


Fig. 2.5: Cross-section and top-down view of typical vertical/substrate BJT device in N-well CMOS process technologies

The vertical PNP transistor, also known as the substrate PNP transistor, is the parasitic PNP of the lateral device. Because its base is relatively wide (approximately equal to the depth of the N-well, which is on the order of few µm), it has lower β than the lateral PNP. Values of β lower than 3 are not uncommon in modern process technologies as seen on Figure 2.1 – this is because in small process nodes the N-well has to be thicker and more doped to prevent punch-through [17, p.27]. On the other hand, because the base current of the vertical PNP tends to be relatively large, its non-ideal higher order components do not affect its value as much as if it were smaller. Wide base also means that the transistor is more resistant to both the forward and reverse Early effects because the induced changes in the width of the depletion region of the base junctions are relatively small compared to the base's width. Current crowding is not an issue in vertical devices either due to their geometry as the current flows vertically and can occupy wide horizontal space, which is the reason for why there is a region of currents where β is nearly current independent. The main disadvantage is, however, obvious – the collector of vertical PNPs is permanently connected to the substrate and therefore to the ground. This makes biasing the transistor via I_C impossible. Biasing the transistor by forcing current into its emitter is the only solution, but low β causes I_C to differ considerably from I_E. This is problematic, because V_{BE} is not determined by I_E but rather by I_C, as evidenced by (2.3). Compensating for low β is therefore required.

Another potential advantage of substrate BJTs comes from the fact that their processing shift might be measurable with on-chip circuitry, which would signifi-

cantly improve untrimmed precision. This process compensation technique relies on the so-called "base pinch" resistor, which is the resistor formed by the N-well between the two base connections on the cross-section shown on Figure 2.5. Its name comes from the base region which is "pinched" by the emitter region (which has to be grounded for proper function). This resistor is significantly voltage dependent and imprecise, which is why it is practically never used, but its resistance is correlated to I_S, which makes sense given how similar the base pinch resistor and the substrate BJT structures are. According to [20] correlation factor of $\rho = 0.81$ has been found in a 130 nm process, though only 6 samples have been measured. In any case, TSMC 110 model library does not include base pinch resistors and while it should be possible to lay them out without violating design rules, it is impossible to simulate them. This thesis will therefore not utilize this technique.

2.2 Bipolar transistor based smart temperature sensor architecture

This section will provide insight into the function of the ADC and the DSP circuits. While these blocks will not be designed in this thesis, it is necessary to understand their function in order to design an analog front-end which is compatible with the conventional architecture of BJT-based temperature sensors. The overall architecture is depicted on Figure 2.6.

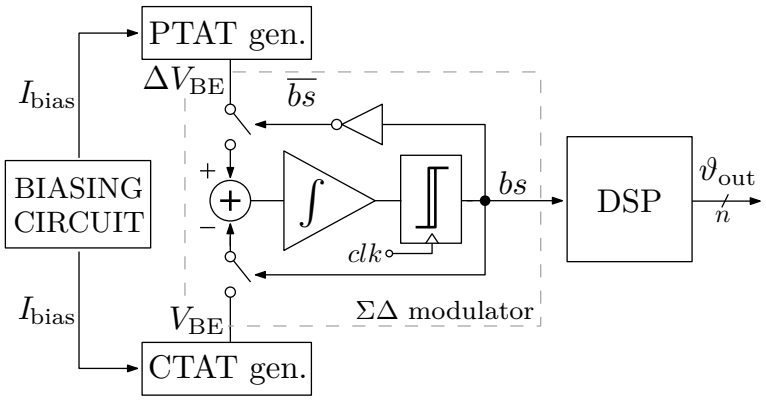


Fig. 2.6: BJT-based smart temperature sensor architecture

2.2.1 ΣΔ modulator

The ΣΔ modulator is an ADC which trades off speed for high precision and resolution, which is why it is the ADC of choice in smart temperature sensors, as was already noted in section 1.1. It consists of an integrator, a comparator, and a

feedback loop which controls the inputs of the modulator, as shown in Figure 2.6. When the output of the comparator *bs* (for bitstream) is logic low, the upper switch is closed and ΔV_{BE} is integrated. This increases the voltage on the integrator's output until the comparator switches to logic high. In this state, the lower switch is closed, therefore *negative* V_{BE} is integrated until the integrator's output drops low enough to switch the comparator back to logic low. This mode of operation is called *charge-balancing* – the charge accumulated during the integration of the positive input is equal to the charge accumulated during the integration of the negative input. It should be noted that the comparator should have its output synchronized to a clock so that the DSP can reliably count the bits of the bitstream.

Because the circuit element which performs the integration is a capacitor in an operational amplifier feedback loop, it has to be charged with current rather than voltage in order to perform integration, as the following well-known equation for voltage across capacitors shows

$$V_{\mathrm{C}}(t) = \frac{1}{C} \cdot \int I_{\mathrm{c}}(t)\, dt \tag{2.10}$$

This means that it is necessary to input currents proportional to the voltages rather than the voltages themselves. The well-known operational amplifier (opamp) integrator circuit on Figure 2.7a converts the voltage to current utilizing the resistor. A more integrated solution is shown on Figure 2.7b where the currents proportional to the compared voltages are fed into the integrator directly. In these circuits the polarity of the signals was reversed relative to Figure 2.6 because these are inverting integrator configurations.

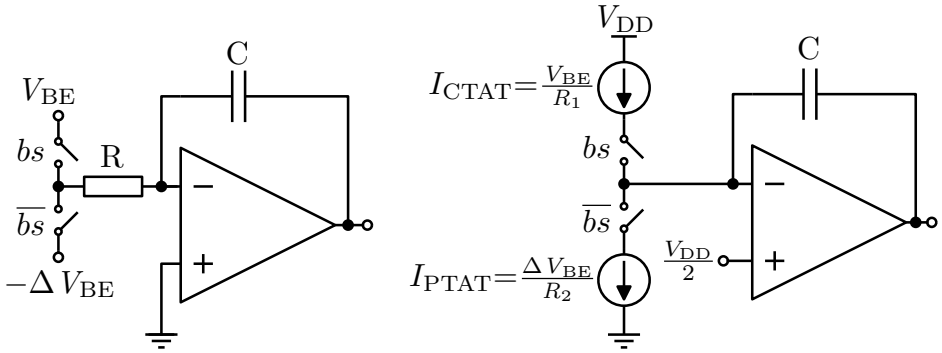


Fig. 2.7: Voltage output inverting integrator implementations

The $\Sigma\Delta$ modulator generates a PDM (pulse-density modulated) 1-bit signal *bs* with an average value of μ. If I_{PTAT} is greater than I_{CTAT}, the integrator's capacitor will charge more rapidly when $bs = 0$ and thus spend less time in this state, and the

average value of the bitstream μ will be therefore closer to 1. The charge-balancing operation can be mathematically described by the following equation:

$$\mu \cdot I_{\mathrm{CTAT}} = (1 - \mu) \cdot I_{\mathrm{PTAT}} \tag{2.11}$$

After rearranging, it is possible to express the average value of the bit-stream μ as a function of the input voltages.

$$\begin{aligned} \mu \cdot (I_{\mathrm{CTAT}} + I_{\mathrm{PTAT}}) &= I_{\mathrm{PTAT}} \\ \mu &= \frac{I_{\mathrm{PTAT}}}{I_{\mathrm{CTAT}} + I_{\mathrm{PTAT}}} \end{aligned} \tag{2.12}$$

Further mathematical rearranging can make familiar expressions from Figure 1.4 appear, assuming the currents are generated by applying the V_{BE} and ΔV_{BE} voltages onto resistors R_1 and R_2.

$$\mu = \frac{\frac{\Delta V_{\mathrm{BE}}}{R_2}}{\frac{V_{\mathrm{BE}}}{R_1} + \frac{\Delta V_{\mathrm{BE}}}{R_2}} = \frac{\frac{R_1}{R_2} \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{BE}} + \frac{R_1}{R_2} \cdot \Delta V_{\mathrm{BE}}} \approx \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{BE}} + \alpha \cdot \Delta V_{\mathrm{BE}}} \approx \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}} \tag{2.13}$$

This finding has important consequences for the designer of the analog front-end. Firstly, it means that α can be set by a ratio of two resistances in voltage-to-current converters. Secondly, it means that the smart temperature sensor does not need to physically produce the V_{REF} voltage – the ADC compares the PTAT signal ΔV_{BE} against V_{REF} implicitly due to the mechanism of its charge-balancing operation. Because μ represents a ratio of a PTAT quantity and a temperature independent quantity, μ itself will be PTAT as well. This is called *ratiometric* measurement.

2.2.2 Digital signal processing

The DSP's role is to filter the digital data with a low pass filter to filter out the quantization noise, decimate the data ($\Sigma\Delta$ modulators are a type of oversampling ADC) and finally convert the data to a useful unit such as degrees Celsius. The conversion is done by a simple equation

$$\vartheta_{\mathrm{out}} = A \cdot \mu + B \tag{2.14}$$

where ϑ_{out} is the result of the measurement in Celsius, and A and B are constants. The value of A tends to be around 500-700 °C, as this is the temperature range over which μ goes from 0 to 1, and B is ideally absolute zero (-273.15 °C). The optimal values of these constants should be determined by simulation for best fit.

As the average value of μ can change during the conversion due to either temperature change or due to employment of time-domain techniques such as chopping or

DEM, incremental DSPs are often used [17, p.120]. One possible and easily understandable way of implementing this mode of operation is using two digital counters in the DSP which are clocked at the same frequency as the output comparator of the $\Sigma\Delta$ modulator. One counter simply counts to a fixed number N while the other counter is enabled by the bitstream and therefore counts the number of ones in the bistream. When the first counter finishes counting, the conversion stops and the total number of ones is compared to the total number of bits N, which represents the average value of μ over the whole conversion time. This means that all the abrupt changes that may happen to μ during the conversion are averaged in the DSP. The counters obviously also serve as decimators, as they output their values only once every N samples.

2.3 Error categorization and sensitivity analysis

This section will provide a categorization and mathematical analysis of errors present in BJT-based temperature sensors.

The most basic way of categorizing errors is described in the following list.

- **Systematic errors**
  Errors which are predictable, the same for all chips and which can be in principle eliminated by design, for example the curvature of V_{BE}.
- **Random errors**
  Unpredictable errors which are zero on average.
  - **Process errors**
    Errors which cause all the devices of the same type on the chip shift the same direction away from their nominal parameters. Sometimes the circuits can be made insensitive to some process errors or the process spread of some components might correlate with some quantities measurable on chip, but these errors are often impossible to eliminate without trimming.
  - **Mismatch**
    Errors which cause identical devices on the same die to differ from each other. These errors can be reduced by making the matched components large due to Pelgrom's law [21], they can also be minimized in layout, and methods such as DEM can be used to average these errors out in the time domain if necessary.

The second way of categorizing errors in BJT-based temperature sensors, which is important for error budgeting, will be shown in subsection 2.3.1 and the third way, which is important for trimming purposes, will be discussed in subsection 2.3.2.

2.3.1 Sensitivity analysis

As the equation for the average value of bitstream consists of V_{BE}, ΔV_{BE} and α as seen in (2.13), it is possible to categorize the errors present in the circuit according to which of these quantities they affect. It is also possible to calculate the sensitivity of the output temperature reading to the errors in these quantities.

The sensitivity of the output quantity to a change in the input quantity S_{in}^{out} is a partial derivative of the output quantity function with respect to the given input quantity. The sensitivity of the temperature reading ϑ_{out} to changes in V_{BE}, ΔV_{BE} and α can be calculated using (2.13) and (2.14) as follows.

$$\begin{aligned} S_{V_{\mathrm{BE}}}^{\vartheta_{\mathrm{out}}} &= \frac{\partial \vartheta_{\mathrm{out}}}{\partial V_{\mathrm{BE}}} = \frac{\partial (A \cdot \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{BE}} + \alpha \cdot \Delta V_{\mathrm{BE}}} + B)}{\partial V_{\mathrm{BE}}} = \\ &= -\frac{A \cdot \alpha \cdot \Delta V_{\mathrm{BE}}}{{V_{\mathrm{REF}}}^2} = -\frac{A \cdot \mu}{V_{\mathrm{REF}}} = -\frac{T}{V_{\mathrm{REF}}} \end{aligned} \tag{2.15}$$

$$\begin{aligned} S_{\Delta V_{\mathrm{BE}}}^{\vartheta_{\mathrm{out}}} &= \frac{\partial \vartheta_{\mathrm{out}}}{\partial (\Delta V_{\mathrm{BE}})} = \frac{\partial (A \cdot \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{BE}} + \alpha \cdot \Delta V_{\mathrm{BE}}} + B)}{\partial (\Delta V_{\mathrm{BE}})} = \frac{A \cdot \alpha \cdot V_{\mathrm{BE}}}{{V_{\mathrm{REF}}}^2} = \\ = \frac{A \cdot \alpha \cdot (V_{\mathrm{REF}} - \alpha \cdot \Delta V_{\mathrm{BE}})}{{V_{\mathrm{REF}}}^2} &= \frac{A \cdot \alpha \cdot (1 - \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}})}{{V_{\mathrm{REF}}}^2} = \frac{\alpha \cdot (A - T)}{V_{\mathrm{REF}}} \end{aligned} \tag{2.16}$$

$$\begin{aligned} S_{\alpha}^{\vartheta_{\mathrm{out}}} &= \frac{\partial \vartheta_{\mathrm{out}}}{\partial \alpha} = \frac{\partial (A \cdot \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{BE}} + \alpha \cdot \Delta V_{\mathrm{BE}}} + B)}{\partial \alpha} = \\ = \frac{A \cdot \Delta V_{\mathrm{BE}} \cdot V_{\mathrm{BE}}}{{V_{\mathrm{REF}}}^2} &= \frac{A \cdot V_{\mathrm{BE}} \cdot \mu}{\alpha \cdot V_{\mathrm{REF}}} = \frac{T \cdot V_{\mathrm{BE}}}{\alpha \cdot V_{\mathrm{REF}}} = \\ = \frac{T}{\alpha} \cdot \frac{V_{REF} - \alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}} &= \frac{T}{\alpha} \cdot \left(1 - \frac{T}{A}\right) \end{aligned} \tag{2.17}$$

The approximation $\mu = \frac{T}{A}$ was used in these derivations, which can be justified by rearranging (2.14).

$$\mu = \frac{\vartheta_{\mathrm{out}} - B}{A} \approx \frac{\vartheta_{\mathrm{out}} + 273.15\,^{\circ}\mathrm{C}}{A} = \frac{T_{\mathrm{out}}}{A} \approx \frac{T}{A} \tag{2.18}$$

It is clearly visible that the sensitivity of the temperature reading to errors in V_{BE} is PTAT, while the sensitivity to ΔV_{BE} is CTAT. Finally the sensitivity to errors in α is at its maximum near the middle of the temperature range.

As the voltage signals are converted into currents so that they can be integrated in the $\Sigma\Delta$ modulator as Figure 2.6 shows, some errors do not affect the voltages and only corrupt the currents, the sensitivity of the output reading to errors in the currents should be therefore calculated as well.

$$\begin{aligned} S_{I_{\mathrm{PTAT}}}^{\vartheta_{\mathrm{out}}} &= \frac{\partial \vartheta_{\mathrm{out}}}{\partial I_{\mathrm{PTAT}}} = \frac{\partial (A \cdot \frac{I_{\mathrm{PTAT}}}{I_{\mathrm{CTAT}} + I_{\mathrm{PTAT}}} + B)}{\partial I_{\mathrm{PTAT}}} = \\ &= A \cdot \frac{I_{\mathrm{REF}} - I_{\mathrm{PTAT}}}{{I_{\mathrm{REF}}}^2} = A \cdot \frac{I_{\mathrm{CTAT}}}{{I_{\mathrm{REF}}}^2} \end{aligned} \tag{2.19}$$

$$S^{\vartheta_{\text{out}}}_{I_{\text{CTAT}}} = \frac{\partial \vartheta_{\text{out}}}{\partial I_{\text{CTAT}}} = \frac{\partial (A \cdot \frac{I_{\text{PTAT}}}{I_{\text{CTAT}}+I_{\text{PTAT}}} + B)}{\partial I_{\text{CTAT}}} = \\ = -A \cdot \frac{I_{\text{PTAT}}}{{I_{\text{REF}}}^2} \tag{2.20}$$

All the previous sensitivity equations will be later used to evaluate the significance of the errors in the sensor and propose approximate specifications for the precision of the sensing circuits in the following chapter.

2.3.2 Temperature dependency of errors

The last important way of categorizing errors in the analog front-end of the temperature sensor is by the nature of their temperature dependence.

- **Temperature independent errors**
  TI errors, also known as offset errors, are often caused by mismatch of components which set important ratios. The most significant TI (or rather nearly TI) error is the input voltage offset of opamps. Other TI errors include spread of β or errors caused by the packaging shift.
- **Linearly temperature dependent errors**
  This class of errors is often synonymous with PTAT errors or gain errors in literature. The most significant of these errors is the PTAT error in V_{BE} caused by the process spread of the saturation current, which was discussed in subsection 2.1.2. The other significant PTAT error is biasing current spread which will be discussed in subsection 3.1.1. These two errors are impossible to eliminate by design and are so large they have to be trimmed out.
- **Higher order / non-linear errors**
  The main error in this class is the systematic curvature of V_{BE} as discussed subsection 2.1.2, though many other factors (some systematic and some random) such as the temperature dependence of β contribute as well [17, p.24]. The overall curvature is nevertheless dominated by the approximately quadratic systematic curvature of V_{BE} which can be compensated for by design. Third order (and higher) components are usually neglected as they are relatively small and significantly more difficult to remove.

This way of categorizing errors is important for the design of the trimming circuits. This is because each trimming operation done at a single trimming temperature can only trim out one of the above mentioned categories of errors while potentially exacerbating others. Trimming strategies will be further described in the following chapter.

3 BIPOLAR TRANSISTOR BASED SMART TEMPERATURE SENSOR CIRCUIT SOLUTIONS

This chapter will describe one possible way of implementing BJT-based smart temperature sensor's analog front-end on a transistor level. It will start by describing the simplest versions of the circuits and analyzing their errors. Advanced circuit techniques used to reduce some of the most significant errors will be discussed afterwards, and finally an improved version of the analog front-end circuits will be presented. The improved circuits will be then implemented in TSMC 110 processing technology in the following chapter 4.

3.1 Simple biasing circuit

The biasing circuit's role is to generate a current which will be used in the sensing circuits to bias the bipolar transistors inside. The current should rise with T^3 in order to compensate for the curvature of V_{BE} as was shown in subsection 2.1.2. As implementing power of three relationship requires complex translinear circuits which utilize regular bipolar transistors (substrate PNPs are not sufficient due to the grounded collector), PTAT biasing current utilizing ΔV_{BE} is the best available solution. The biasing current should also be process and supply voltage independent.

A simple version of the most common ΔV_{BE}-based biasing circuit is depicted on Figure 3.1. Similar biasing circuit has been used in other implementations such as [8], [9], [17, p.250], [24] or [25] as this is basically the best currently known circuit solution. The PMOS bulk connections are not depicted, as in this thesis they will be connected to the supply voltage (V_{DD}) unless noted otherwise.

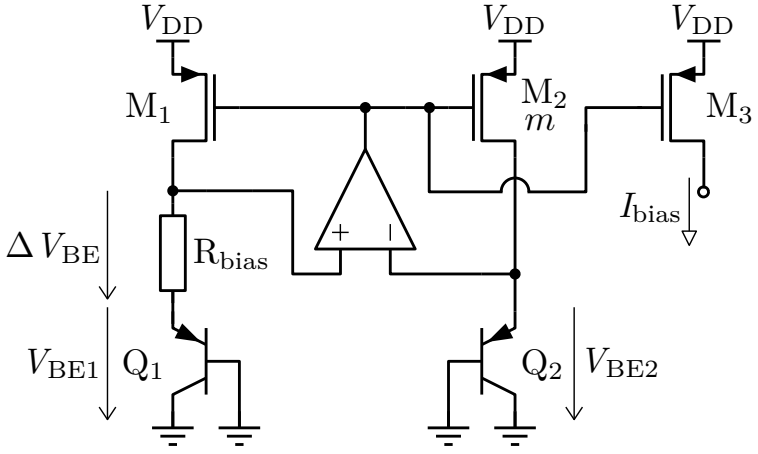


Fig. 3.1: Simple biasing circuit

The PMOS transistors $M_{1\text{-}3}$ driven by the opamp form current sources where M_2 biases the substrate PNP transistor Q_2 with m-times the current that flows through M_1. This is ensured by making the aspect ratio ($\frac{W}{L}$) of M_2 m-times larger than the $\frac{W}{L}$ of M_1. The V_{BE} voltage of Q_1 will therefore be somewhat larger than the V_{BE} of Q_1 as its emitter current is m-times greater. The opamp negative feedback loop sets the currents in the branches so that the voltages at the opamp inputs are equal, therefore the difference between the two V_{BE} voltages is directly applied to the resistor R_{bias}. The current that flows in the left branch is then simply determined by Ohm's law and (2.5) as follows

$$I_{\mathrm{bias}} = \frac{\Delta V_{\mathrm{BE}}}{R_{\mathrm{bias}}} = \frac{kT \cdot \ln m}{q \cdot R_{\mathrm{bias}}} \tag{3.1}$$

and it can be easily used to bias the sensing BJTs by simply mirroring it with additional PMOS transistors such as M_3.

Depending on the TCR of the resistor, the biasing current can be made temperature independent (if the TCR is positive and large enough) or, in case of negative TCR, the current can follow a steeper temperature dependency than PTAT, which is desirable as this leads to smaller curvature of V_{BE} as was proven in subsection 2.1.2. While large positive TCR resistors such as the n-well based resistors are available in CMOS processing technologies, large negative TCR is unavailable. Polysilicon resistors are the only resistors with a slightly negative TCR, the high resistance version having more negative TCR than the normal version, as seen on Figure 1.2. While the high resistance polysilicon resistor represents additional processing costs, the shallower curvature, increased precision and reduced area can be more valuable.

There are several errors in the biasing circuit depicted on Figure 3.1 and these errors will be examined in the following subsections. These errors manifest themselves as errors in the biasing current. The PTAT signal ΔV_{BE} is not affected by errors in the biasing current because it is defined by a ratio of the biasing currents instead (as was proven in subsection 2.1.1), but V_{BE} is affected, which is why it is important to diminish the errors in the biasing circuit as much as possible.

3.1.1 Resistance process spread

The largest error in the biasing circuit is caused by the process spread of the resistor's resistance. In TSMC 110, the polysilicon resistors spread by approximately $\pm 5\%/\sigma$. This spread manifests itself as an equivalent spread in the generated biasing current. The error in V_{BE} generated by a biasing current which is subject to process spread can be calculated as follows

$$V_{\mathrm{BE}} = \frac{kT}{q} \ln \frac{I_{\mathrm{C}} + \varepsilon(I_{\mathrm{C}})}{I_{\mathrm{S}}} = \frac{kT}{q} \cdot \left[\ln \left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}} \right) + \ln \left(1 + \frac{\varepsilon(I_{\mathrm{C}})}{I_{\mathrm{C}}} \right) \right] \tag{3.2}$$

$$\varepsilon(V_{\mathrm{BE}}) = \frac{kT}{q} \ln\left(1 + \frac{\varepsilon(I_{\mathrm{C}})}{I_{\mathrm{C}}}\right) \tag{3.3}$$

As (3.3) shows, the error introduced by the resistance process spread is PTAT. The term $\frac{\varepsilon(I_{\mathrm{C}})}{I_{\mathrm{C}}}$ represents the relative error in I_{C}. Assuming 3σ spread, an approximation of the error can be calculated at the top of the temperature range ($T \approx 400\,\mathrm{K}$), where the error is the largest.

$$\varepsilon(V_{\mathrm{BE}}) = \frac{kT}{q} \ln\Big(1 + \delta(I_{\mathrm{C}})\Big) = \frac{k \cdot 400}{q} \ln\Big(1 + 3 \cdot (\pm 5\%)\Big) = \pm 4.82\,\mathrm{mV} \tag{3.4}$$

Using the sensitivity of the temperature reading to errors in V_{BE} as derived in (2.15), equivalent temperature reading error at the top of the temperature range can be calculated.

$$\varepsilon(\vartheta_{\mathrm{out}}) = S_{V_{\mathrm{BE}}}^{\vartheta_{\mathrm{out}}} \cdot \varepsilon(V_{\mathrm{BE}}) = -\frac{T}{V_{\mathrm{REF}}} \cdot \varepsilon(V_{\mathrm{BE}}) = -\frac{400}{1.2} \cdot (\pm 4.82 \cdot 10^{-3}) \approx \pm 1.61\,^{\circ}\mathrm{C} \tag{3.5}$$

An error contribution of $\pm 1.6\,^{\circ}\mathrm{C}$ is unacceptably high, however as there is no reliable way to predict the process spread of the resistors, the only possible way to reduce this error is trimming.

3.1.2 Operational amplifier errors

The operational amplifier brings two errors into the circuit – an error caused by its finite open loop gain A_{OL}, and its input voltage offset V_{offset}. The input voltage offset is random as it is caused by mismatch of the internal opamp components and it directly adds to the amplified signal (ΔV_{BE} in this case). The finite open loop gain causes the voltage at the opamp inputs to differ by a small amount. This amount is equal to the output signal of the opamp divided by its gain and this systematic input voltage offset adds to the amplified signal in the same way as the random offset, they can be therefore analyzed in the same way.

The error in V_{BE} caused by this kind of error can be derived as follows, assuming that $\varepsilon(\Delta V_{\mathrm{BE}}) \ll \Delta V_{\mathrm{BE}}$ which allows the approximation $\ln(1 + x) = x$.

$$\begin{aligned} V_{\mathrm{BE}} &= \frac{kT}{q} \ln\left(\frac{\Delta V_{\mathrm{BE}} + \varepsilon(\Delta V_{\mathrm{BE}})}{R_{\mathrm{bias}} \cdot I_{\mathrm{S}}}\right) = \\ &= \frac{kT}{q}\left[\ln\left(\frac{\Delta V_{\mathrm{BE}}}{R_{\mathrm{bias}} \cdot I_{\mathrm{S}}}\right) + \ln\left(1 + \frac{\varepsilon(\Delta V_{\mathrm{BE}})}{\Delta V_{\mathrm{BE}}}\right)\right] \end{aligned} \tag{3.6}$$

$$\varepsilon(V_{\mathrm{BE}}) \approx \frac{kT}{q} \cdot \frac{\varepsilon(\Delta V_{\mathrm{BE}})}{\Delta V_{\mathrm{BE}}} = \frac{\varepsilon(\Delta V_{\mathrm{BE}})}{\ln m} \tag{3.7}$$

Utilizing (2.15), the equivalent temperature reading error caused by the opamp offset errors is defined by the following equation.

$$\varepsilon(\vartheta) = S_{V_{\mathrm{BE}}}^{\vartheta_{\mathrm{out}}} \cdot \varepsilon(V_{\mathrm{BE}}) = -\frac{T}{V_{\mathrm{REF}}} \cdot \frac{\varepsilon(\Delta V_{\mathrm{BE}})}{\ln m} \tag{3.8}$$

As the equation above shows, while the error in V_{BE} can be TI (opamp gain usually drops off at higher temperatures but random input voltage offset tends to be relatively stable), the resulting error in the temperature reading is nevertheless PTAT, as the sensitivity of V_{BE} to errors is PTAT as well.

Assuming that the temperature reading error contribution of these two errors should be less than $\pm 0.1\,^{\circ}\mathrm{C}$ and $m = 5$, specification for the opamp offsets can be derived.

$$\varepsilon(\Delta V_{\mathrm{BE}}) < \frac{\varepsilon(\vartheta_{\mathrm{out}}) \cdot V_{\mathrm{REF}} \cdot \ln m}{T} = \frac{\pm 0.1 \cdot 1.2 \cdot \ln 5}{400} \approx \pm 483\,\mu\mathrm{V} \tag{3.9}$$

Achieving 3σ random input voltage offset lower than $\pm 0.5\,\mathrm{mV}$ may be possible in some mature process technologies with careful layout, but the size of the components in the opamp would have to be rather large. More efficient way of achieving offset this small is some form of offset cancellation such as chopping, which will be discussed later.

As for the open loop gain, it should satisfy the following equation

$$A_{\mathrm{OL}} > \frac{V_{\mathrm{out}}}{\varepsilon(\Delta V_{\mathrm{BE}})} \tag{3.10}$$

The voltage at the output of the opamp is $V_{\mathrm{DD}} - V_{\mathrm{GS}}$ as it drives a PMOS transistor. Assuming $V_{\mathrm{DD}} = 3\,\mathrm{V}$ and $V_{\mathrm{GS}} = 1\,\mathrm{V}$, the necessary open loop gain can be calculated.

$$A_{\mathrm{OL}} > \frac{V_{\mathrm{DD}} - V_{\mathrm{GS}}}{\varepsilon(\Delta V_{\mathrm{BE}})} = \frac{3-1}{483 \cdot 10^{-6}} \approx 4140 \approx 72\,\mathrm{dB} \tag{3.11}$$

The specifications derived in this chapter should be only understood as rough estimates so that the designer can decide which approach to take.

3.1.3 Current ratio error

Mismatch of the current mirror will cause error in the current ratio m. This error will modify the ΔV_{BE} generated across the biasing resistor. The approximation $\ln(1+x) = x$ for small x has been used again.

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q} \ln\Big(m + \varepsilon(m)\Big) = \frac{kT}{q}\left[\ln(m) + \ln\left(1 + \frac{\varepsilon(m)}{m}\right)\right] \tag{3.12}$$

$$\varepsilon(\Delta V_{\mathrm{BE}}) \approx \frac{kT}{q} \cdot \frac{\varepsilon(m)}{m} \tag{3.13}$$

This error is PTAT and it directly adds to ΔV_{BE} just as the errors caused by the opamp and the specification for $\delta(m)$ can be derived in the same way, utilizing the result of (3.7). Assuming $m = 5$, maximum error contribution of $\pm 0.1\,^{\circ}\mathrm{C}$ and $T = 125\,^{\circ}\mathrm{C}$ for tightest bound, the matching requirement can be calculated.

$$\varepsilon(V_{\mathrm{BE}}) \approx \frac{\varepsilon(\Delta V_{\mathrm{BE}})}{\ln m} \tag{3.14}$$

$$\varepsilon(\vartheta_{\text{out}}) = S_{V_{\text{BE}}}^{\vartheta_{\text{out}}} \cdot \varepsilon(V_{\text{BE}}) = -\frac{T}{V_{\text{REF}}} \cdot \frac{\varepsilon(\Delta V_{\text{BE}})}{\ln m} = -\frac{T}{V_{\text{REF}}} \cdot \frac{\frac{kT}{q} \cdot \delta(m)}{\ln m} \tag{3.15}$$

$$\delta(m) < \frac{q \cdot \varepsilon(\vartheta_{\text{out}}) \cdot V_{\text{REF}} \cdot \ln m}{kT^2} = \frac{q \cdot (\pm 0.1) \cdot 1.2 \cdot \ln 5}{k \cdot 400^2} \approx \pm 0.014 = \pm 1.4\% \tag{3.16}$$

Matching of around ±1% is possible with medium-to-large sized transistors. However if error contribution of less than ±0.01 °C was required, the matching of the transistors would need to be better than ±0.14%, which is practically impossible to achieve without matching improving techniques such as DEM.

3.2 Simple sensing circuits

There are two sensing circuits – the PTAT and the CTAT generators with V-to-I (voltage to current) converters. These circuits will be presented and analyzed together as some errors are caused by the relative matching of these two circuits.

3.2.1 Simple CTAT generator

The role of the CTAT generator is self explanatory – it should produce an accurate V_{BE} voltage using the biasing current and convert this voltage into a current which will serve as an input for the ΣΔ modulator in accordance with the findings mentioned in subsection 2.2.1. Its simplest and most common implementation is depicted on Figure 3.2, nearly identical to solutions used in [9], [17, p.234] or [25].

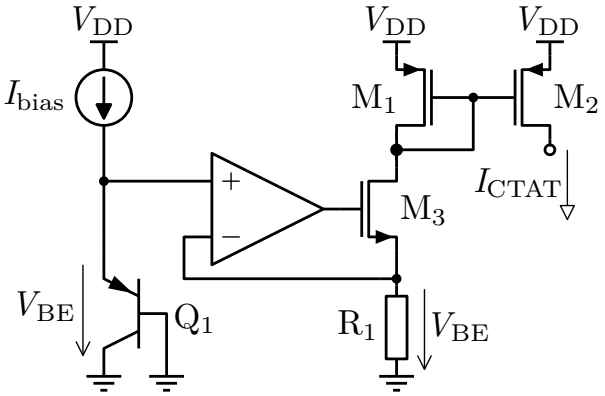


Fig. 3.2: Simple CTAT generator

The bulk connection of M_3 is not shown as the bulks of NMOS transistors are irreversibly connected to the substrate and therefore to circuit ground by the nature of common n-well based CMOS process technologies including TSMC 110.

The opamp's feedback ensures that the V_{BE} voltage is copied across the resistor R_1 and therefore directly generates a CTAT current. The PMOS current mirror $\text{M}_{1\text{-}2}$ copies the current from the current sinking output of the V-to-I converter (the

drain of M_3) to a current sourcing output (the drain of M_2). The output node of the mirror can therefore be directly connected to the $\Sigma\Delta$ modulator.

3.2.2 Simple PTAT generator

The circuit depicted on Figure 3.3 is a type of ΔV_{BE} generator with a V-to-I converter integrated into the structure, as seen in [17, p.233]. The output node can be directly connected to the $\Sigma\Delta$ modulator according to Figure 2.7b.

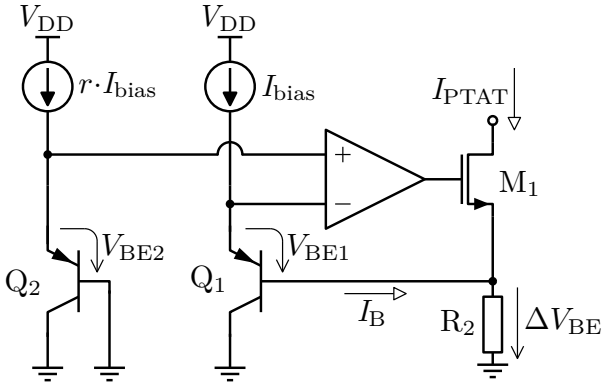


Fig. 3.3: Simple PTAT generator

As the feedback loop keeps the voltages at the inputs of the opamp equal, the difference between the two V_{BE} voltages develops across the resistor R_2, which generates a PTAT current. The V-to-I converter is therefore integrated in the feedback loop.

3.2.3 Saturation current spread

This type of error only affects the V_{BE} generator (ΔV_{BE} should be independent of I_{S} as was shown in subsection 2.1.1) and it was already analyzed in subsection 2.1.2. In this subsection an estimation of the temperature reading error caused by the spread of saturation current will be calculated using the sensitivity equation (2.15) and the spread of V_{BE} depicted on Figure 2.2, which is approximately $\pm 8\,\mathrm{mV}$ at $125\,^{\circ}\mathrm{C}$.

$$\varepsilon(\vartheta_{\mathrm{out}}) = S_{V_{\mathrm{BE}}}^{\vartheta_{\mathrm{out}}} \cdot \varepsilon(V_{\mathrm{BE}}) = -\frac{T}{V_{\mathrm{REF}}} \cdot \varepsilon(V_{\mathrm{BE}}) = -\frac{400}{1.2} \cdot (\pm 8 \cdot 10^{-3}) \approx \pm 2.67\,^{\circ}\mathrm{C} \quad (3.17)$$

This is the largest error present in the circuit by far and if some kind of process compensation is not possible (as explained in subsection 2.1.3) it is necessary to reduce it by trimming.

3.2.4 Operational amplifier errors

The opamp errors – the systematic offset of the finite gain and the random input offset voltage – affect the sensing circuits more significantly than the biasing circuit. In the case of both sensing circuits, these errors directly apply to the amplified signals, which are V_{BE} and ΔV_{BE} respectively.

Assuming $\alpha = 10$, $A = 600\,\mathrm{K}$ and desired error contribution of less than $\pm 0.1\,^{\circ}\mathrm{C}$, the offset of the opamps should satisfy the following conditions derived using the sensitivity equations (2.15) and (2.16). The temperature which would lead to tightest precision constraint was chosen – this means 400 K for the V_{BE} error and $-50\,^{\circ}\mathrm{C}$ or 220 K for the ΔV_{BE} error.

$$\varepsilon(V_{\mathrm{BE}}) < \frac{\varepsilon(\vartheta_{\mathrm{out}})}{S^{\vartheta_{\mathrm{out}}}_{V_{\mathrm{BE}}}} = \frac{\varepsilon(\vartheta_{\mathrm{out}}) \cdot V_{\mathrm{REF}}}{T} = \frac{\pm 0.1 \cdot 1.2}{400} = 300\,\mu\mathrm{V} \tag{3.18}$$

$$\varepsilon(\Delta V_{\mathrm{BE}}) < \frac{\varepsilon(\vartheta_{\mathrm{out}})}{S^{\vartheta_{\mathrm{out}}}_{\Delta V_{\mathrm{BE}}}} = \frac{\varepsilon(\vartheta_{\mathrm{out}}) \cdot V_{\mathrm{REF}}}{\alpha \cdot (A - T)} = \frac{\pm 0.1 \cdot 1.2}{10 \cdot (600 - 220)} \approx 32\,\mu\mathrm{V} \tag{3.19}$$

It is clearly impossible to reach random input offset voltages this small without offset cancellation techniques.

As for the opamp gain, its minimum value for error contribution $\pm 0.1\,^{\circ}\mathrm{C}$ can be calculated after the output voltage of the opamps is known. For the CTAT generator, the output voltage is $V_{\mathrm{BE}} + V_{\mathrm{GS}}$, while for the PTAT generator, its about $\Delta V_{\mathrm{BE}} + V_{\mathrm{GS}}$. Naturally, the lower the V_{GS} the better – here, the worst case estimates $V_{\mathrm{BE}} \approx 0.8\,\mathrm{V}$, $V_{\mathrm{GS}} \approx 0.8\,\mathrm{V}$ and $\Delta V_{\mathrm{BE}} \approx 80\,\mathrm{mV}$ will be used.

$$A_{\mathrm{OL\ CTAT}} > \frac{V_{\mathrm{BE}} + V_{\mathrm{GS}}}{\varepsilon(V_{\mathrm{BE}})} = \frac{0.8 + 0.8}{300\,\mu\mathrm{V}} \approx 5333 \approx 74.5\,\mathrm{dB} \tag{3.20}$$

$$A_{\mathrm{OL\ PTAT}} > \frac{\Delta V_{\mathrm{BE}} + V_{\mathrm{GS}}}{\varepsilon(\Delta V_{BE})} = \frac{0.08 + 0.8}{32\,\mu\mathrm{V}} \approx 29333 \approx 89\,\mathrm{dB} \tag{3.21}$$

Gain this high is only achievable with cascodes and large transistors, or with two stage opamps. As the opamps in both biasing and sensing circuits drive capacitive loads, single stage high output impedance opamps would be more easily stabilized, but if the gain was still insufficient, two stage opamp would be necessary, which would bring potential stability problems. Large value of Miller capacitance could be required to achieve reasonable phase margin, and the capacitor could end up being so large area-wise that the benefit of smaller transistor two-stage opamp would be lost. Finding a suitable opamp topology is an important task for the designer.

3.2.5 Current ratio and bipolar transistor mismatch errors

These errors are only present in the ΔV_{BE} generator and are caused either by mismatch of the current sources (error in the r current ratio) or by mismatch of the

bipolar transistors themselves. As substrate bipolar transistors tend to match relatively well, its mostly the current sources which are of concern, but both effects behave in the same way. Assuming $\varepsilon(r) \ll r$, the error can be expressed as follows

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q} \ln\Big(r + \varepsilon(r)\Big) = \frac{kT}{q}\Big[\ln(r) + \ln\Big(1 + \frac{\varepsilon(r)}{r}\Big)\Big] \tag{3.22}$$

$$\varepsilon(\Delta V_{\mathrm{BE}}) \approx \frac{kT}{q} \cdot \frac{\varepsilon(r)}{r} \tag{3.23}$$

This error is PTAT and its effect on the output temperature reading can be evaluated using the sensitivity equation for ΔV_{BE} errors (2.16), assuming $r = 9$ and maximum error contribution of $\pm 0.1\,^{\circ}\mathrm{C}$. It may be interesting to note that while the error itself is PTAT, the sensitivity is CTAT, which means the largest error contribution happens near the middle of the temperature range ($\approx 300\,\mathrm{K}$).

$$\varepsilon(\vartheta_{\mathrm{out}}) = S^{\vartheta_{\mathrm{out}}}_{\Delta V_{\mathrm{BE}}} \cdot \varepsilon(\Delta V_{\mathrm{BE}}) = \frac{\alpha \cdot (A - T)}{V_{\mathrm{REF}}} \cdot \frac{kT}{q} \cdot \delta(r) \tag{3.24}$$

$$\delta(r) < \frac{q \cdot V_{\mathrm{REF}} \cdot \varepsilon(\vartheta_{\mathrm{out}})}{k \cdot T \cdot \alpha \cdot (A - T)} = \frac{q \cdot 1.2 \cdot (\pm 0.1)}{k \cdot 300 \cdot 10 \cdot (600 - 300)} \approx 0.155\% \tag{3.25}$$

Such accuracy of matching of MOS transistors is impossible without DEM.

3.2.6 Errors in the gain factor α

Errors in the PTAT signal scale factor α can come from two different sources – the mismatch of the resistors R_1 and R_2 which set α as was shown in (2.13), and the mismatch of the transfer ratio of the current mirror at the output of the V_{BE} generator depicted on Figure 3.2. This is because if, for example, the current mirror transferred only half of the generated I_{CTAT} current to the $\Sigma\Delta$ modulator, α would be effectively doubled. Indeed it is possible to implement α solely this way and it may be actually preferable to using the resistance ratio for reasons which will be described later. In any case, both effects cause the same result – α is affected by a random error, which is most significant near the middle of the temperature range.

The precision of α assuming maximum error contribution of $\pm 0.1\,^{\circ}\mathrm{C}$ can be calculated using the sensitivity equation (2.17).

$$\varepsilon(\alpha) \cdot S^{\vartheta_{\mathrm{out}}}_{\alpha} = \varepsilon(\vartheta_{\mathrm{out}}) \tag{3.26}$$

$$\varepsilon(\alpha) < \frac{\varepsilon(\vartheta_{\mathrm{out}})}{\frac{T}{\alpha} \cdot (1 - \frac{T}{A})} \tag{3.27}$$

$$\delta(\alpha) < \frac{\varepsilon(\vartheta_{\mathrm{out}})}{T \cdot (1 - \frac{T}{A})} = \frac{\pm 0.1}{300 \cdot (1 - \frac{300}{600})} = \frac{1}{1500} \approx 0.066\% \tag{3.28}$$

As the above result shows, the temperature reading is highly sensitive to any spread of α, which should be made as precise as possible. DEM should be employed for both the resistors and the current mirror, regardless of which one of these components actually sets α. If the resistors were exactly identical and large enough area-wise, it may be possible to sufficiently match them without DEM in layout with the most precise layout techniques (inter-digitized layout, plenty of dummy devices etc.), but then implementing DEM of the current mirror is absolutely crucial.

It is important to mention that potential difference in the voltages at the drains of the current mirror transistors can cause systematic error in α as well. This is caused by the finite output impedance of the MOS transistor in saturation. Cascode current mirror can be used to reduce this error significantly. In other current mirrors of the analog front-end, such as the biasing circuit or the ΔV_{BE} generator, the finite output impedance errors should not be as pronounced because the opamps ensure the same voltages at the drains of the current mirrors, but nevertheless cascoding them as well is beneficial, because it helps to keep the gain of the feedback loops high and the systematic offset low.

3.2.7 Bipolar transistor current gain β errors

There are two kinds of error associated with β – its process spread and its temperature dependence. If the circuits were designed to be insensitive to β, both of these effects would stop affecting the precision of the circuit altogether.

The CTAT generator on Figure 3.2 is affected by β because V_{BE} is set by the collector current, but the transistor is biased by the emitter current. This causes V_{BE} to be β dependent. This is especially problematic because the β of substrate bipolar transistors is so low.

$$\begin{aligned} V_{\mathrm{BE}} &= \frac{kT}{q} \ln \frac{I_{\mathrm{C}}}{I_{\mathrm{S}}} = \frac{kT}{q} \ln \frac{I_{\mathrm{bias}} - I_{\mathrm{B}}}{I_{\mathrm{S}}} = \\ &= \frac{kT}{q} \ln \frac{I_{\mathrm{bias}} - \frac{I_{\mathrm{bias}}}{\beta+1}}{I_{\mathrm{S}}} = \frac{kT}{q} \ln \left(\frac{I_{\mathrm{bias}}}{I_{\mathrm{S}}} \cdot \frac{\beta}{\beta+1} \right) \end{aligned} \tag{3.29}$$

If the biasing current was made to be dependent on $\frac{\beta+1}{\beta}$, the terms would cancel out and V_{BE} would become β independent.

The PTAT generator on Figure 3.3 is β dependent as well, though in a different way. Because there is a non-zero base current of Q_1 flowing through the resistor R_2, it subtracts from the current I_{PTAT}. If the voltage across the resistor was greater than ΔV_{BE} by just the right amount to account for the base current, the I_{PTAT} current would be unaffected.

Both of these errors can be fixed by implementing a single additional resistor. In the case of making the biasing current $\frac{\beta+1}{\beta}$ dependent, a resistor of the right value

can be inserted into the base of the transistor Q_2 in the biasing circuit to achieve this dependence, as depicted on Figure 3.4.

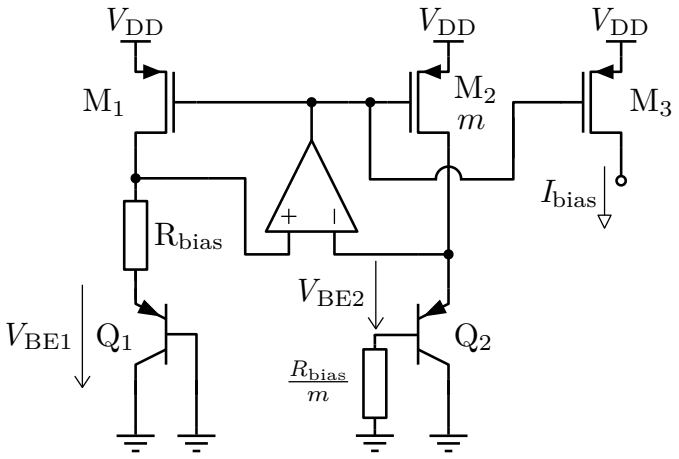


Fig. 3.4: Simple biasing circuit with finite β compensation

This is a commonly used circuit solution and has been applied or mentioned in [8], [17, p.92-95], [23], [24] and many other implementations.

The feedback loop still keeps the voltages at the opamp's inputs the same. This can be described by the following equation

$$V_{\mathrm{BE1}} + I_{\mathrm{bias}} \cdot R_{\mathrm{bias}} = V_{\mathrm{BE2}} + I_{\mathrm{B2}} \cdot \frac{R_{\mathrm{bias}}}{m} \tag{3.30}$$

The biasing current I_{bias} can be expressed after rearranging.

$$V_{\mathrm{BE1}} + I_{\mathrm{bias}} \cdot R_{\mathrm{bias}} = V_{\mathrm{BE2}} + \frac{m \cdot I_{\mathrm{bias}}}{\beta + 1} \cdot \frac{R_{\mathrm{bias}}}{m} \tag{3.31}$$

$$I_{\mathrm{bias}} \cdot R_{\mathrm{bias}} - \frac{I_{\mathrm{bias}} \cdot R_{\mathrm{bias}}}{\beta + 1} = V_{\mathrm{BE2}} - V_{\mathrm{BE1}} \tag{3.32}$$

$$I_{\mathrm{bias}} = \frac{\Delta V_{\mathrm{BE}}}{R_{\mathrm{bias}}} \cdot \frac{\beta + 1}{\beta} \tag{3.33}$$

The biasing current β dependence described in (3.33) is precisely the one needed to cancel out the β dependence of V_{BE}.

As for the ΔV_{BE} generator, a similar solution can be used, as seen on Figure 3.5 and presented in [17, p.233].

The function of the additional resistor is most easily described mathematically. The negative feedback configuration of the opamp ensures its inputs are at the same voltage relative to ground. Solving the equation for the I_{PTAT} current shows that it is now β independent, as the β-dependent terms cancel out.

$$\begin{aligned} V_{\mathrm{BE1}} + I_{\mathrm{PTAT}} \cdot R_2 + \frac{I_{\mathrm{bias}}}{\beta + 1} \cdot R_2 &= V_{\mathrm{BE2}} + \frac{r \cdot I_{\mathrm{bias}}}{\beta + 1} \cdot \frac{R_2}{r} \\ I_{\mathrm{PTAT}} = \frac{V_{\mathrm{BE2}} - V_{\mathrm{BE1}}}{R_2} &= \frac{\Delta V_{\mathrm{BE}}}{R_2} \end{aligned} \tag{3.34}$$

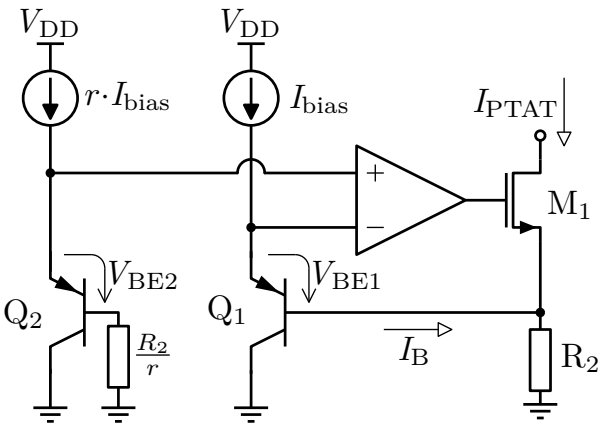


Fig. 3.5: Simple ΔV_{BE} generator circuit with finite β compensation

3.3 Advanced circuit techniques

This section will present the forementioned advanced circuit techniques which will be implemented into the circuits in order to reduce some of the errors described in the previous sections.

3.3.1 Chopping

Chopping is an offset cancellation technique which effectively modulates the random input voltage offset of an opamp by a periodical signal to separate it from the original DC (or rather nearly DC) signal. Then it can be filtered or averaged out in the time or frequency domains, while the original signal is left unaffected. The principle of operation is shown on Figure 3.6.

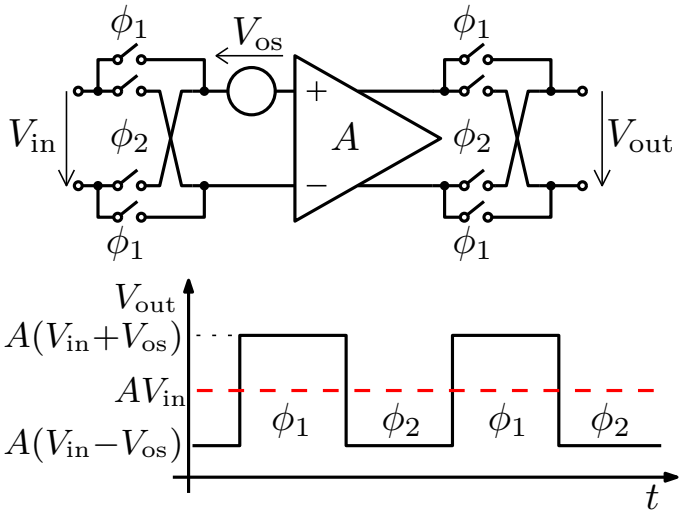


Fig. 3.6: Chopper amplifier principle of operation

In the first phase of chopping ϕ_1 the outer switches are closed, while in the second phase ϕ_2 the inner switches are closed. As the polarity of the input signal is periodically reversed by the input switches, the input signal V_{in} is effectively modulated by a square wave. Random input offset voltage V_{os} is added to the modulated input signal, which is then amplified by the amplifier. The amplified signal is then modulated once again at the output of the amplifier by the very same square wave. The modulated amplified input signal AV_{in} is therefore demodulated, while the input voltage offset is modulated by the square wave for the first time. This causes the output voltage to oscillate between $A(V_{\text{in}} + V_{\text{os}})$ and $A(V_{\text{in}} - V_{\text{os}})$. The average value of the output signal is obviously AV_{in}, i.e. the amplified signal without the offset error, and this average value can be reconstructed with a low-pass or averaging filter.

In short, the chopping technique works because the input signal is modulated twice, while the input voltage offset is modulated only once. This essentially separates the offset from the input signal in the frequency domain.

There are some constraints and requirements for this technique to work. The switching phases ϕ_1 and ϕ_2 have to be equally long, i.e. the clock that drives the switches has to have 50% duty cycle. As the chopping technique is also capable of reducing the opamp noise, the chopping frequency should be higher than the corner frequency of the $1/f$ noise, so that most of this noise is modulated and separated from the input voltage signal as well. However, as the chopping frequency increases, the inevitable transient spikes caused by charge injection and clock feed-through effects [22] become more dominant simply because they happen more often.

The residual offset of chopper amplifiers caused by the transient spikes is usually on the order of few µV. If lower offset is required, chopping can be employed twice (so-called *nested chopping* technique), or in this particular case, the $\Sigma\Delta$ modulator can be disconnected from the analog-front end during the transient spike period (so-called *guard time* technique) [17, p.199].

It should be noted that chopping is particularly suited for implementation in systems with incremental $\Sigma\Delta$ modulator, as the DSP following the modulator can average out the offset (and the noise) as described in subsection 2.2.2. This means that no analog filtering of the oscillating output signal is required.

3.3.2 Dynamic Element Matching

Dynamic Element Matching is a time-domain technique used to average out mismatch errors of identical devices. It can be used when a number of identical circuit elements perform some function – most often setting a ratio of some kind – which should be as precise as possible. The elements can be periodically interchanged so

that every possible configuration of the elements is active once during the full DEM cycle. Averaging the output signal over time yields a signal which is significantly more precise, as mismatch between the elements is nearly completely eliminated.

The mathematical proof will be explained on an example of dynamically matched current sources which set the r current ratio in the ΔV_{BE} generator circuit. Figure 3.7 illustrates this for $r = 9$, which means 10 unit elements (current sources) and therefore 10 steps in the DEM cycle.

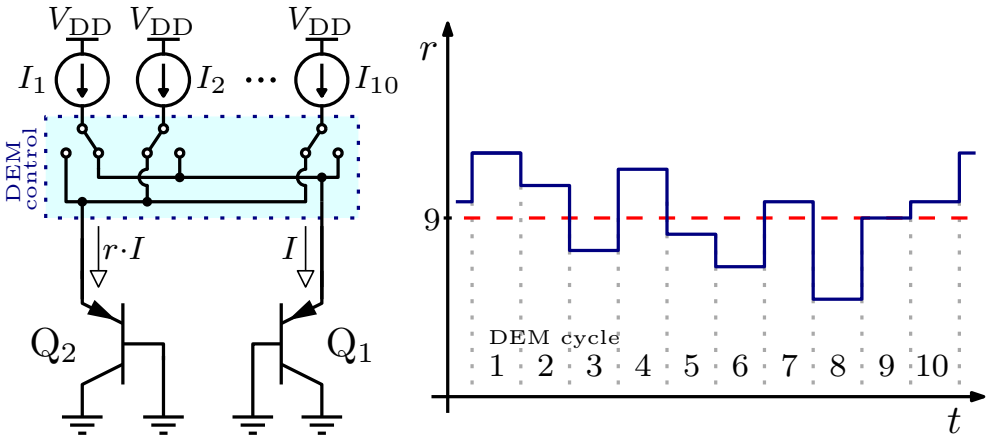


Fig. 3.7: Example of dynamic current source matching in ΔV_{BE} generator

The error in r manifests itself as an error in ΔV_{BE} as explained in subsection 3.2.5. Previously an approximation for $\ln(1+x)$ was used – if $x \ll 1$, the logarithm amounts to approximately x. This time, more accurate Taylor series expression will be used so that a more accurate estimate for the remaining error after DEM is obtained.

$$\varepsilon(\Delta V_{\mathrm{BE}}) = \frac{kT}{q} \ln\Big(1 + \delta(r)\Big) = \frac{kT}{q}\Big[\delta(r) - \frac{1}{2}\delta(r)^2 + \frac{1}{3}\delta(r)^3 - ...\Big] \tag{3.35}$$

As the DEM algorithm is essentially summing all the mismatch related errors and averaging them over time, the average error can be expressed as follows

$$\begin{aligned} \overline{\varepsilon(\Delta V_{\mathrm{BE}})} &= \frac{1}{r+1} \cdot \frac{kT}{q} \cdot \sum_{i=1}^{r+1} \Big[\delta(r)_i - \frac{1}{2} \cdot \delta(r)_i^2 + \frac{1}{3} \cdot \delta(r)_i^3 - ...\Big] = \\ &= \frac{1}{r+1} \cdot \frac{kT}{q} \cdot \Big\{ \sum_{i=1}^{r+1} \delta(r)_i + \sum_{i=1}^{r+1} \Big[- \frac{1}{2} \cdot \delta(r)_i^2 + \frac{1}{3} \cdot \delta(r)_i^3 - ...\Big]\Big\} \end{aligned} \tag{3.36}$$

Since mismatch is a random error and its mean value is 0, the following equation can be written

$$\sum_{i=1}^{r+1} \delta(r)_i = 0 \tag{3.37}$$

which can be combined with (3.36) to receive the following

$$\overline{\varepsilon(\Delta V_{\mathrm{BE}})} = \frac{1}{r+1} \cdot \frac{kT}{q} \cdot \sum_{i=1}^{r+1} \Big[-\frac{1}{2} \cdot \delta(r)_i^2 + \frac{1}{3} \cdot \delta(r)_i^3 - ... \Big] \tag{3.38}$$

This shows that DEM essentially removes the first order errors. The improvement is significant. Assuming that the mismatch of the current sources is 1%, the maximum error of ΔV_{BE} without DEM is approximately 343 µV, while with DEM, it is only 2 µV. This is equivalent to matching better than 0.01%.

An important condition for DEM to work is to ensure that the inputs do not change during the cycle. The inputs in the case of the ΔV_{BE} generator DEM are the current sources themselves – if the biasing current were to change in the middle of the cycle, the mismatch error would not be eliminated. Therefore the DEM cycles have to get successively faster so that they are not disrupted by changing inputs. With three or four successive DEM algorithms, the control frequencies required could get very high and it is not possible to just apply DEM to everything mindlessly. If chopping is implemented in the circuit, it should be controlled by the slowest clock and all the DEM cycles have to happen during both chopping phases – chopping should be two times slower than the slowest DEM cycle.

Just as chopping, DEM is well suited for applications with incremental ΣΔ ADCs which perform the averaging in the digital domain.

3.3.3 Ratiometric curvature compensation

Ratiometric curvature compensation (a term coined in [17, p.88]) compensates the concave curvature inherent to V_{BE} by utilizing the fact that the temperature reading is done by measuring a ratio of two quantities, as explained in subsection 2.2.1, and by exploiting the negative *TCR* of the resistors used.

Previously it was assumed that the sum of the PTAT and CTAT signals V_{REF} (or more accurately I_{REF} as the signals are converted into currents) should be a TI signal and the value of the PTAT signal gain factor α would be picked to accomplish that. However, the goal is not to design a reference signal but rather a linear function of temperature. Finding the value of α which leads to most linear I_{REF} rather than to the least temperature dependent one is a better strategy. The value of α which accomplishes this is usually larger than the one which would lead to a temperature independent sum. This is because there is a slight convex curvature to I_{PTAT}, which is caused by the negative *TCR* of the polysilicon biasing current defining resistor. It should also be noted that by converting V_{BE} to I_{CTAT} a small amount of its concave curvature is compensated as well simply because of the negative *TCR*.

However, finding the correct value of α for the most linear I_{REF} does not mean that μ is going to be most linear as well, as seen on Figure 3.8, where $\alpha = 7$

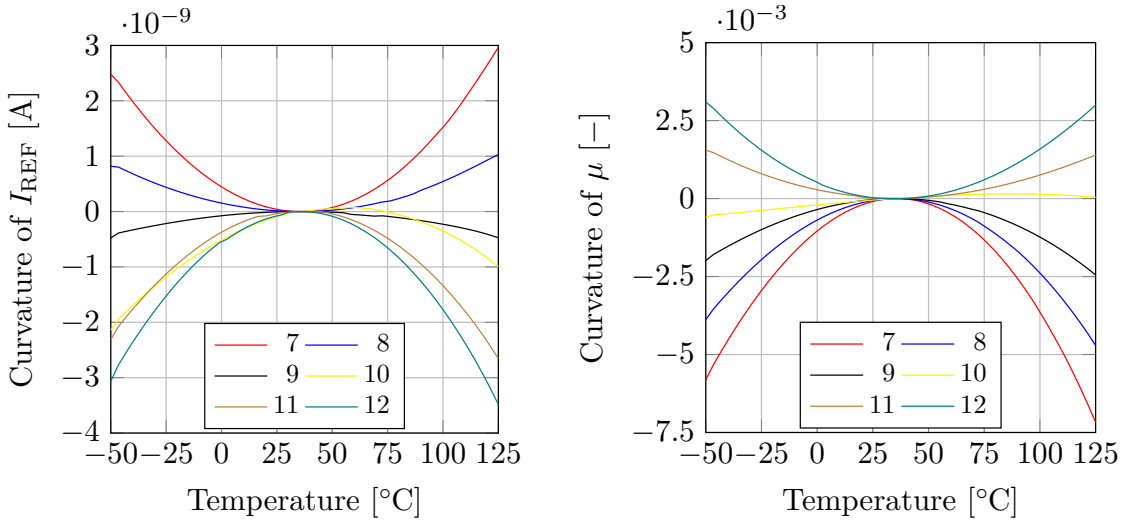


Fig. 3.8: Example simulated curvature of I_{REF} and μ for different values of α

would lead to most TI I_{REF}, but $\alpha = 9$ leads to most linear I_{REF} and $\alpha = 10$ leads to most linear μ (this is just an example – the precise values of α depend on m, r, the resistor TCR and the bipolar devices themselves). This is because $\mu = I_{\mathrm{PTAT}}/I_{\mathrm{REF}}$ and as was mentioned, I_{PTAT} has convex curvature. Finding the value of α which ensures that μ is as linear as possible utilizing parametric sweeps in the circuit simulator is therefore the best design procedure. Implementing this curvature correction technique leads to relatively small non-linearity of the output temperature reading without needing any special circuitry and should be satisfactory for most applications.

3.3.4 Trimming

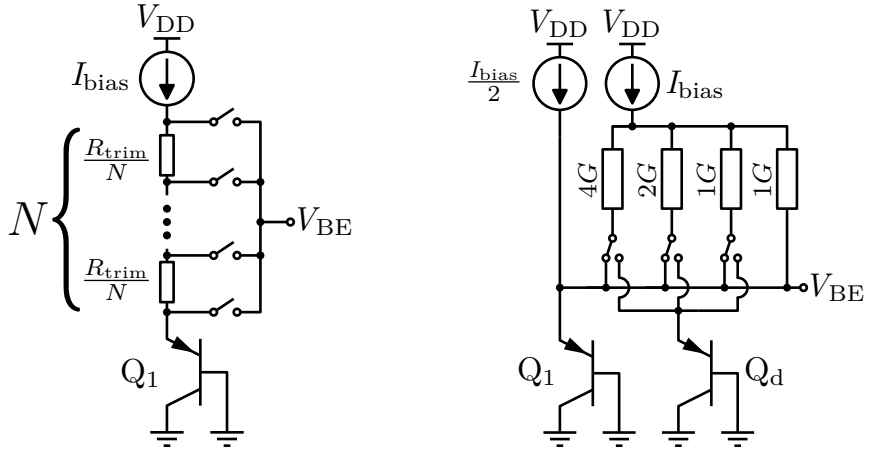
As the errors caused by the biasing current spread (due to resistance processing spread) and the spread of I_{S} are very large and irremovable otherwise, trimming needs to be employed. Because both of these errors affect V_{BE} only, it makes sense to trim V_{BE} only, and as both errors are PTAT (as proven in subsection 2.1.2 and subsection 3.1.1), a PTAT trim is needed.

To clarify, PTAT trim is a trim which adds a variable quantity to V_{BE} which is linearly temperature dependent. For example, the equation

$$V_{\mathrm{BE\,trim}} = V_{\mathrm{BE}} + \kappa \cdot T \cdot V_{\mathrm{trim}} \tag{3.39}$$

describes a PTAT trim, assuming κ represents a tuneable correction factor which controls how much of V_{trim} is going to be added to V_{BE}. This additional PTAT quantity should be able to compensate for the PTAT spread of V_{BE}. In order to be able to effectively subtract from V_{BE} in case it is too high, the default value of κ has

to be non-zero. It should be also noted that for the PTAT trim to be most effective, other types of errors (TI and higher order ones, as described in subsection 2.3.2) should be minimal and only PTAT errors should be present in the circuit. This is because a PTAT trim cannot correct for other types of errors and these errors can be exacerbated by a PTAT trim in some parts of the temperature range.



(a) Variable resistor trimming (b) Variable current trimming

Fig. 3.9: Example of two V_{BE} trimming methods

There are many ways of adding a variable PTAT voltage to V_{BE}. The most obvious one is depicted on Figure 3.9a where a variable resistor is used. This resistor is made up of N resistor segments with $N+1$ taps. As the current flowing through the resistor ladder is PTAT, the voltage drop across the resistors is PTAT as well. There are several limitations to this method. Firstly, only one of those taps can be active at the same time, i.e. only one switch can be closed – otherwise a part of the resistance ladder is shorted and current flows through the switches, which can cause voltage drop across the switch which has non-zero $R_{DS\,on}$. If only one tap is active at a time, even large values of $R_{DS\,on}$ (and therefore small switches) are satisfactory because no current is flowing through the switches. Second limitation is the fact that the trimming code is most likely stored as a binary number, while the number of taps is 2^n+1 where n is the number of bits. This means there needs to be a digital decoder from binary to one-hot encoding, which along with the interconnect routing takes up significant area, as achieving for example 5 bits of trimming resolution requires 32 resistors and 33 switches.

An alternative method of trimming is shown on Figure 3.9b. A current divider serves to divide the biasing current into binary-weighted parts (other methods of weighing are of course also possible) and depending on the position of the switches, the current is either sent into the sensing transistor, or into a dummy transistor. In the example on Figure 3.9b, the current can be varied from $\frac{5}{8} \cdot I_{bias}$ to $\frac{3}{2} \cdot I_{bias}$ in

7 steps with only three bits, three switches and no decoder needed. Many ratios, combinations and weighing schemes can be implemented this way with relatively few switches. The switches themselves can be small as their voltage drop is not sensed along with V_{BE}, which is advantageous as well. The main limitation is that the currents always have to flow through the divider, and if the current is not needed in the sensing transistor, it has to be redirected to the dummy transistor, as otherwise if one of the divider's paths was disconnected, the input current would not divide into binary weighed parts and V_{BE} would be corrupted. Alternatives to dummy transistor include analog ground circuits (the voltage at the emitter of Q1 can be copied by a buffer with low impedance output capable of sinking) or connecting the unused current to ground via additional cascoding stages. This is because the current dividers are in fact implemented with PMOS transistors with varying $\frac{W}{L}$ (which sets the weighing) and a difference in the voltage at their drains would manifest itself as a difference in the drain currents which would corrupt the trimming accuracy.

Additional methods of trimming V_{BE} includes trimming by connecting more bipolar transistors in parallel with the original one which achieves an increase of emitter area and therefore a decrease in the current density flowing through the transistor. The switches have to be large, however, as the voltage drop $R_{\mathrm{DS\,on}}$ adds to V_{BE}, substrate bipolar transistors in general tend to be rather large as well and it is hard to achieve fine trimming without sacrificing significant area. It is however possible to combine this method with the previous ones – the MSB of the trimming code can control the additional bipolar transistor while the other bits can control the resistors, the biasing currents etc.

As trimming can be thought of as a form of digital-to-analog conversion (DAC), mismatch between the trimming elements (the resistors in the case of Figure 3.9a and the current dividing MOS transistors in the case of Figure 3.9b) manifests itself as a differential non-linearity (DNL) in the DAC transfer function, i.e. the discrete steps by which V_{BE} can change depending on the trimming code are not all equally large depending on the matching. If the desired value of V_{BE} happens to lie in the middle of a step, the remaining error after trimming can be as large as half the step, good matching therefore minimizes the maximum potential residual error after trimming. This is a potential advantage of the resistor trimming method, as resistors tend to match better than MOS transistors.

Trimming is usually done at a single temperature point as heating the chips, letting them settle at at the chosen temperature and trimming them is costly. If the trimming is done on wafer before dicing, the wafer more easily and quickly reaches the same temperature in its whole volume, while if the trimming is done after dicing and packaging, the packaging shift can be trimmed out too, but the chips have

higher thermal capacity and they can have different temperature at the start of the process which means there needs to be enough time for all the chips to settle at the target trimming temperature.

To hasten the trimming process, two additional bipolar transistors biased at a known current ratio can be implemented on the chip – as ΔV_{BE} is well defined, temperature of the chip can be calculated from the ΔV_{BE} measurement practically instantly and trimming can be therefore done anytime at any temperature. This, however, requires additional bond pads or probe pads on the chip, additional bipolar transistors with additional current sources etc. The trimming temperature also has an effect on the residual error after trimming and its choice is not arbitrary, which will be explained along with the design of the trimming circuit in the following chapter 4.

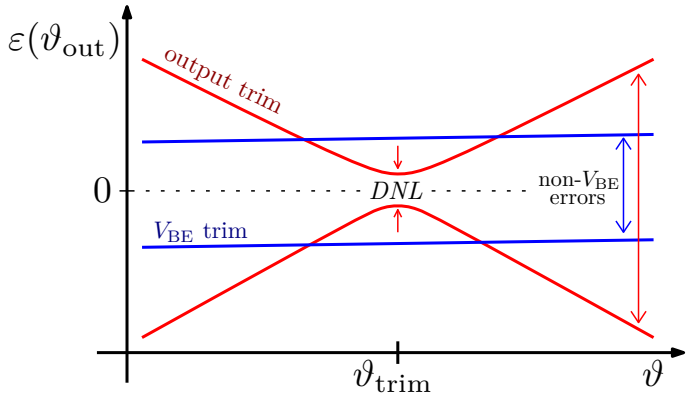


Fig. 3.10: Comparison of the trimming methods based on the trimmed quantity

Finally, there are two ways of how the trimming code can be determined, as shown on Figure 3.10. The obvious way is to find the trimming code which leads to smallest amount of temperature measurement error, $\varepsilon(\vartheta_{\mathrm{out}})$. This type of trim is called the output trim, as the trimming code is determined by measuring the output of the sensor. Output trim forces the temperature error at the trimming temperature $\vartheta_{\mathrm{trim}}$ to be close to zero (residual spread at the trimming temperature is directly proportional to DNL), but while V_{BE} is the dominant source of error in the circuit, it is not the sole one. Therefore this way of trimming is essentially trying to fix all errors, even the ones not associated with V_{BE}, by tuning V_{BE}. This only eliminates those unrelated errors near the trimming temperature $\vartheta_{\mathrm{trim}}$. Applying PTAT trim to solve unrelated and non-PTAT type of errors may end up exacerbating the non-PTAT errors toward the ends of the temperature range.

The other method is to find the trimming code by measuring V_{BE} and trimming it to some fixed known ideal value, usually its modus at the given trimming temperature $\vartheta_{\mathrm{trim}}$. This only solves the V_{BE} related errors and does not affect the other

types of errors present in the circuit, therefore the temperature reading error at the trimming temperature ϑ_{trim} is not forced to be zero. However, this type of trimming does not affect the non-PTAT errors in the circuit, which makes the error spread more evenly over the temperature range.

The second way of trimming requires that the V_{BE} signal is measurable, therefore either auxiliary testability analog muxes and test pins are needed to access this voltage if the trimming is done after packaging, or at least a probe pad is needed if the trimming is done on wafer level. However, if the temperature sensor is expected to experience wide range of temperatures, this is the best method. If, however, the additional testing structures are unavailable, or if the sensor is expected to be working near the trimming temperature most of the time, the first type of trimming may be more economic.

Theoretically, if the V_{BE} caused errors were the only errors present in the sensor, it should not matter which trimming method is chosen. The difference between the methods is only visible when errors unrelated to V_{BE} are not fully eliminated, which is usually the case in real designs.

3.4 Improved front-end circuits

In this section, improved versions of the simple circuits which include the previously discussed advanced circuit techniques will be briefly presented.

3.4.1 Improved biasing circuit

An improved version of the biasing circuit is depicted on Figure 3.11. Aside from DEM and a chopped opamp, the circuit also includes a current mirror $M_{1\text{-}2}$ used for biasing the PMOS cascodes and for generating a "byproduct" voltage $V_{\text{bias N}}$ which can be used to bias NMOS transistors in the sensing circuits when needed. Finally, on the left, there is a starting circuit formed by transistors $M_{5\text{-}7}$ which functions as a current comparator. Even if the circuit is in its off state and no biasing current flows, M_7 is always on. Because no current flows through M_5 when it is off, no current flows through M_7 either and instead it pulls down the voltage at the gate of M_6, which pulls down the voltage $V_{\text{bias P}}$. This makes the biasing circuit turn on and biasing current starts flowing. Once the circuit is on, M_5 turns on as well and starts conducting current. If it is large enough and therefore capable of sourcing sufficiently larger current than M_7 is capable of sinking, the voltage at the gate of M_6 rises significantly, which turns it off. The starting circuit is thus disconnected from the circuit once its role has been fulfilled and it does not affect the biasing circuit anymore.

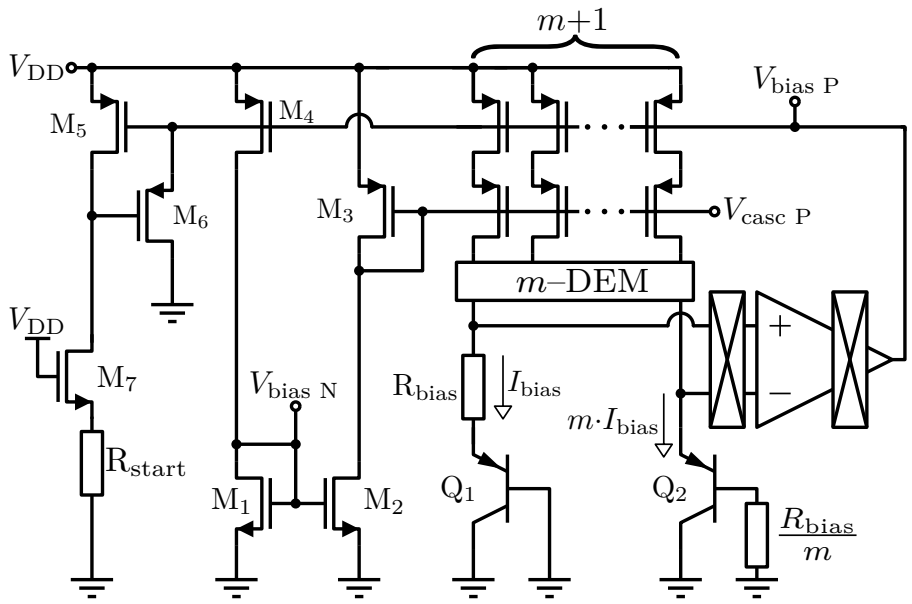


Fig. 3.11: Improved biasing circuit

3.4.2 Improved CTAT generator

An improved version of the CTAT generator is depicted on Figure 3.12. This circuit copies the biasing current using the voltages $V_{\text{bias P}}$ and $V_{\text{casc P}}$ and uses this current to bias the bipolar transistor. The V_{BE} is trimmed by a PTAT trimming block as discussed previously in subsection 3.3.4 and then copied by the chopped opamp onto a resistor, which generates a current $\alpha \cdot I_{\text{CTAT}}$. This current is later divided by α in the dynamically matched current mirror before being transferred to the $\Sigma\Delta$ modulator. Looking at μ, dividing the CTAT signal is equivalent to multiplying the

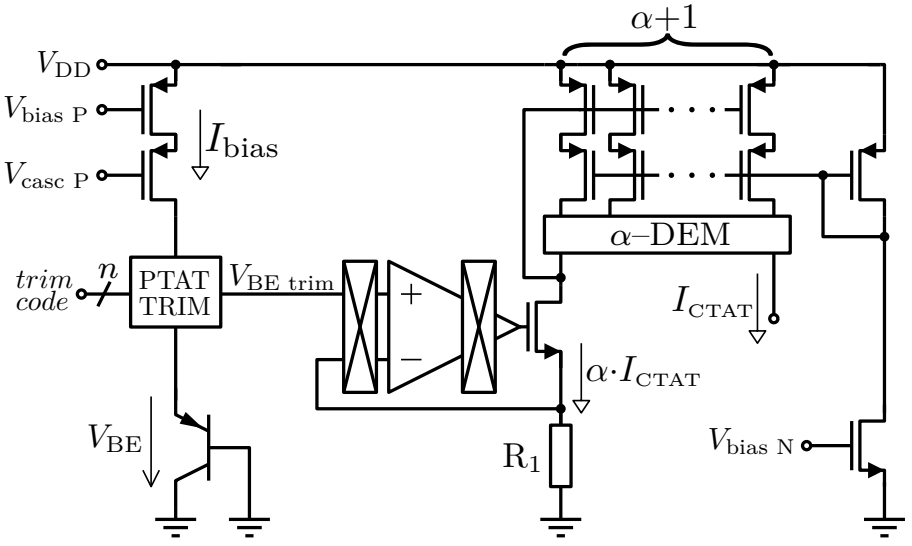


Fig. 3.12: Improved CTAT generator

PTAT signal, as the following equation proves, which means that no scaling of the I_{PTAT} current is needed.

$$\mu = \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{BE}} + \alpha \cdot \Delta V_{\mathrm{BE}}} \cdot \frac{\frac{1}{\alpha}}{\frac{1}{\alpha}} = \frac{\Delta V_{\mathrm{BE}}}{\frac{V_{\mathrm{BE}}}{\alpha} + \Delta V_{\mathrm{BE}}} \tag{3.40}$$

This allows the resistors in the V-to-I converters of the sensing circuits to be identical, which improves their matching.

As is depicted, the cascoded α-implementing current mirror is biased by a structure which utilizes the $V_{\mathrm{bias\ N}}$ voltage from the biasing circuit.

3.4.3 Improved PTAT generator

An improved version of the PTAT generator is depicted on Figure 3.13. There is no significant change from Figure 3.5 aside from cascoded and dynamically matched current sources which set the r current ratio and the chopped opamp.

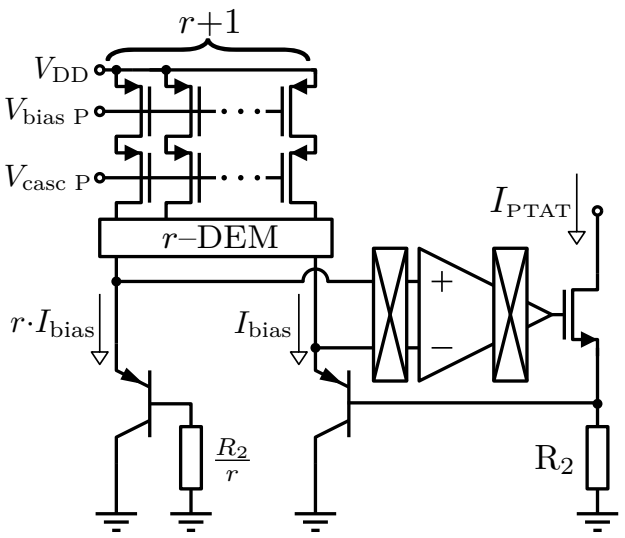


Fig. 3.13: Improved PTAT generator

4 BIPOLAR ANALOG FRONT-END DESIGN IN TSMC 110 PROCESS TECHNOLOGY

This chapter will provide a brief description of the TSMC 110 process technology and will continue by describing the design of a bipolar analog front-end in this particular technology utilizing the techniques outlined in previous chapter 3. Finally, the performance of the design will be evaluated by computer simulation, analyzed and compared with the current state of the art realizations.

4.1 TSMC 110 process technology overview

The manufacturing technology TSMC 110 is an example of a standard n-well based CMOS process. The name of the technology comes from the smallest gate length of the 1.2 V transistor, which is 110 nm. There are also 3.3 V transistors available (*nmos3v* and *pmos3v*) which can be used up to 3.63 V and which are better suited for analog purposes, though their minimum size is not as small (the minimum $W \times L$ is 0.15×0.385 µm for NMOS and 0.15×0.33 µm for PMOS). These MOS devices will be used by default in the subsequent design.

The processing technology offers two bipolar devices: the vertical *vpnp* device as seen on Figure 2.5, and an NPN device manufactured using deep n-well technology. This device, however, requires additional lithographic masks and doping operations due to the deep n-well layer which isolates the transistor from the substrate. Lateral bipolar device is unavailable in this technology. This thesis will use the *vpnp* device for reasons outlined in subsection 2.1.3, which is available in three different sizes labeled by their emitter area: 2×2, 5×5 and 10×10 µm. Because the emitter is the central terminal of the vertical device (as seen on Figure 2.5), the device is actually significantly larger than these numbers suggest. The following design will exclusively use the 5×5 µm emitter area device *vpnp5*, which actually occupies a square of 19×19 µm in layout.

There are many types of resistors available, notable ones include *rphpoly* (P-doped unsalicided polysilicon resistor) and *rphripoly* (a higher sheet resistance version of *rphpoly* requiring extra process steps but approximately 3 times as resistive as *rphpoly*). The minimum recommended resistor width is 1 µm as thinner resistors, while technically feasible, have not been characterized. Available capacitors include Metal-Oxide-Metal (MOM) capacitors, MOS capacitors or Metal-Insulator-Metal (MIM) capacitors. MIM and MOM capacitors tend to be the most precise but also least area efficient, while MOS capacitors have high capacitance per area but are less accurate and less linear. MIM capacitors also require extra process steps and MOM

capacitors take up several metal layers, making them somewhat incompatible with IP core approach as global routing above an IP core which utilizes top metal layers for implementing capacitors would be severely restricted. As the only capacitors in this design will be used for feedback loop compensation where the precision and linearity is not as important, MOS capacitors will be used exclusively.

For some applications native NMOS transistors *nmos3vn* can be desirable. These NMOS transistors are made in the very lightly doped substrate layer instead of heavily doped P-well such as *nmos3v*. Their V_{th} is therefore slightly negative which makes them a suitable solution for some problems caused by insufficient voltage headroom. In this process technology they require no extra process steps.

The Process Design Kit (PDK) comes with process corner device models and process and mismatch Monte Carlo statistical models. Unfortunately, analyses such as *dcmatch* or sensitivity analysis were disabled in the used version of the PDK. Several effects which affect the precision of the designed analog front-end are not modeled, namely the spread of resistor *TCR* coefficients, and some effect are most likely modeled incorrectly, such as the β current dependence as was discussed in subsection 2.1.1.

4.2 Bipolar analog front-end circuit design

In this section, the circuit design of the analog front-end will be described. First, specifications and some system level considerations will be presented. Afterwards, each following subsection will be dedicated to one part of the analog front-end. The design process will be mostly described in chronological order, though the actual design process is rather iterative than straightforward and a lot of fine-tuning changes to previously designed blocks are based on the simulated behavior of the latter blocks.

4.2.1 Design specifications and system level design considerations

As no particular specification is outlined in the goal of this thesis (the limits of what is achievable is mostly given by the technology and not the designer anyway), the design will simply try to achieve the best possible accuracy while not sacrificing disproportionate die area to achieve it – in other words, the design will be approached as if this was an IP core designed for use in SoC ASICs, where a balance between precision and area is paramount. As such, power-down circuits will also be implemented so that the master digital circuit can turn this IP core off when not in use so that power consumption is minimized. There will be only one single temperature

PTAT trim available, as this is in-line with most industrial specifications. The nominal V_{DD} of this design has been chosen to be 3 V as the recent trend is to decrease supply voltages, but the design will function with both higher and lower voltages than that – the upper limit is given by the technology (3.63 V), while the lower limit will depend on the design itself and will have to be found out by simulation.

Military temperature range (−55 °C to 125 °C) has been selected as the default temperature range for which the design will be optimized, as this is the widest conventional temperature range. Lately automotive chips are being designed for temperatures as large as 200 °C. At temperatures this high, leakage currents are more than significant and a different architecture (perhaps forgoing the current mode approach completely) would have to be chosen. It is also a matter of the technology – TSMC 110 is not characterized at temperatures this extreme. In fact, temperatures lower than −40 °C are problematic as well as far as the model trustworthiness goes.

Timing considerations also affect the design of the analog front-end. While the conversion time is in principle flexible (it depends on the speed of DEM and chopping, which can be altered in the digital domain), some nominal value should be chosen for this design. Conversion times ranging from 10 to 100 ms are the most frequent ones in published art. Longer time allows for slower DEM and chopping clocks or for more full DEM and chopping cycles to be run during the conversion, which minimizes the noise, charge injection and clock-feedthrough error contribution, but it increases the average power consumption. In this design, chopping frequency of 20 Hz was chosen to be the nominal value, which also directly determines the frequency of all the DEM cycles as soon as the number of the dynamically matched elements is known. This means that the conversion can be as short as 50 ms if one full chopping and DEM cycle is run during the conversion.

The most important system-level design parameters which affect the whole design and which cannot be unambiguously determined by any design equations are the parameters m (biasing circuit current ratio), r (PTAT generator current ratio) and α (PTAT multiplication, respectively CTAT division factor). In published art, values as low as 3 and as large as 26 are found for these parameters. The choice of value for one of these parameters affects the design quite significantly. For example, if r is high, ΔV_{BE} voltage is rather large and thus α can be smaller etc. These parameters affect the sizes of the resistors for given currents or power consumption criteria, therefore they also affect the area. The number of DEM cycles is also directly proportional to the values of these parameters, which may be important for the design of the digital circuits which drive the DEM algorithms and for overall timing considerations. The values of these parameters also depend on the curvature of V_{BE} and the curvature of the PTAT and CTAT generator resistor's TCR, as ultimately, the values of r and α have to be chosen to ensure that the the temperature

dependency of the average value of the ADC output bitstream (2.12) is as linear as possible.

As was illustrated above, it is hard to determine which values lead to best performance of the sensor, especially in the case of r and α. In the case of m, its value does not have to directly affect r and α, as the biasing resistor can be sized to produce any biasing current based on this ratio, therefore this parameter at least can be more easily determined based on area, timing and error considerations and the thought process behind it is described later in subsection 4.2.3. In this design, initial guess for r and α was made (values which were in the middle part of the range), and the final values $r = 9$ and $\alpha = 10$ were found iteratively using a simplified semi-idealized model of the analog front-end, which used ideal opamps and current mirrors, but real resistors or bipolar transistors.

4.2.2 Chopped operational amplifier design

As the analog-front end will uses three opamps, designing only one opamp good enough for all three use cases is desirable.

Since the opamps drive MOS gates, i.e. capacitive loads, the opamp topology should be ideally single stage with high impedance output as this would make stabilization easy. Simultaneously, it should have high gain and relatively wide output range, as in the case of ΔV_{BE} generator, the output voltage of the opamp is approximately only one V_{GS} above ground, while in the case of the biasing circuit, the situation is exactly opposite. Folded cascode opamp as shown on Figure 4.1 is therefore the topology of choice.

A PMOS input differential pair was chosen because in all three cases, the input common mode voltage is approximately V_{BE}, which ranges from 0.8 to 0.4 V based on temperature. This is relatively low voltage and NMOS differential pair would not have worked properly.

The blue box outlines a second stage. This stage is only necessary for the ΔV_{BE} generator opamp - this is because its output tends to be significantly lower than that of the other opamps (only ΔV_{BE}+V_{GS} above ground). This follower stage therefore serves as a level shifter and helps to keep the cascodes in saturation region in all PVT corners. Either way the compensation capacitor is connected to the high impedance output node of the cascode stage so that a low frequency pole is formed.

The differential pair transistors M_{1-2} are the only PMOS transistors in the sensor whose bulk is connected to the source. This connection improves the common mode rejection ratio ($CMRR$) and power supply rejection ratio ($PSRR$) of the opamp.

The cascode transistors M_{9-12} are connected to the supply rails and they are only in saturation in some PVT corners, especially if the supply voltage is at its

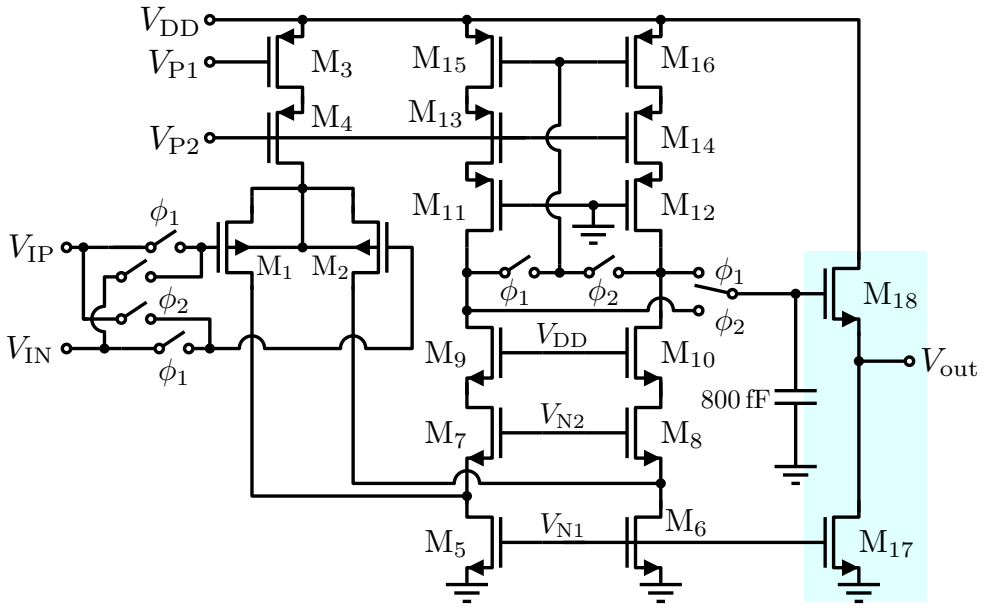


Fig. 4.1: Folded cascode chopped operational amplifier

highest (near 3.63 V) or if the output is close to ground or V_{DD}, when they serve to distribute the voltage more evenly so that channel punchthrough is prevented. Otherwise they are in linear region and do not contribute to the gain significantly.

The voltages V_{P1}, V_{P2}, V_{N1} and V_{N2} have to be generated somewhere for the circuit to work. This is done with auxiliary biasing circuit depicted on Figure 4.2, which uses a biasing current input to produce these voltages. This biasing current can be the same current as generated by the biasing circuits – it is relatively precise and the PTAT temperature dependence may be beneficial because as the temperature rises, the g_m of the transistors that form the opamp will decrease, which will in turn decrease the gain-bandwidth product (GBW). Increasing the biasing current at higher temperature can compensate for this as the g_m will rise along with increasing biasing current. It should be noted, however, that this does not mean that the temperature induced drop off of the DC gain will be compensated for – on the contrary, the gain will drop even more rapidly, because at higher temperatures the biasing current will rise, leading to lower values of r_{ds} of the transistors. The exact reason for why increasing g_m by increasing current will not compensate for the falling gain is such that the g_m rises with square root of current while the output impedance falls with the inverse of current, which is steeper and therefore dominant. This is however not problematic because it does not matter if the gain is temperature dependent, it only matters whether it is large enough so that the systematic offset is low.

Picking the exact value of the biasing current is a matter of compromise. Higher biasing current values leads to higher slew rate and GBW, but the power consump-

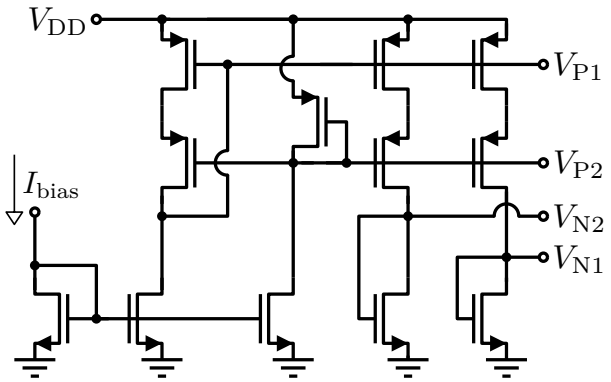


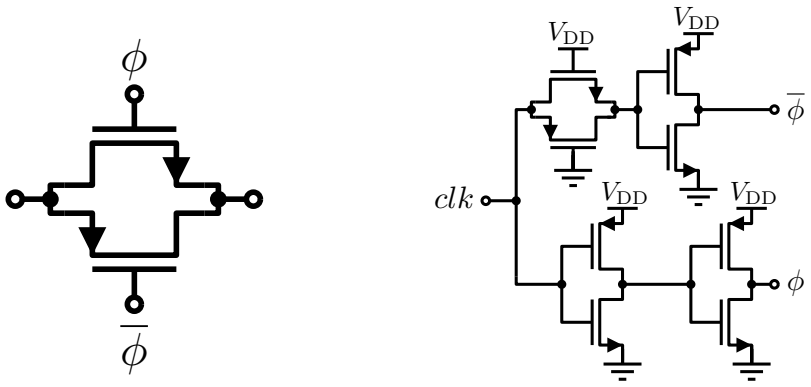
Fig. 4.2: Operational amplifier biasing circuit

tion obviously rises as well and the gain is worse due to reasons outlined above. As neither the slew rate nor the GBW of this opamp are critical (V_{BE} is not expected to change rapidly), biasing current of 1 µA has been chosen in this design. The advantage of such a low current is that it is easy to bias the input differential pair in moderate or even weak inversion where their g_m/I_D efficiency is the highest and where the voltage matching is better as well [26, p.235]. The output impedance of all transistors is also higher if the currents are small. On the other hand, current mirrors match worse in sub-threshold region and they have to be rather long to increase their overdrive and achieve good current matching [26, p.330].

The output chopping modulation is integrated into the opamp so that fully differential output is not actually needed, though the input switches are indeed the same cross configuration as depicted on Figure 3.6. The switches themselves are implemented as analog pass gates or transmission gates as shown on Figure 4.3a, i.e. with two parallel transistors, one of each type. This ensures that it is capable of bi-directionally passing both signals close to ground or to the supply rail, as NMOS is good at passing low voltages and PMOS the large voltages. The voltages in the middle of the voltage range are the ones which are passed the worst through the gate, as neither of those transistors is fully open and some R_{DSon} remains, but as the switches do not actually pass DC current aside from dynamic effects such as gate capacitance charging, the transistors can be minimum size.

As the pass gate switches require both the chopping clock and its inverse signal, a clock inverter circuit is required. Because inverter gate has some delay associated to it, a structure shown on Figure 4.3b is used to ensure that the clocks transition at the same time. This is done using an always open pass gate which approximates the inverter delay without actually inverting the signal. The sizing of these MOS transistors is minimum as well.

Power-down switches were implemented in several places of the opamp so that the opamp draws no current when off and the gates of all transistors are at a well defined



(a) Analog pass gate (b) Clock inverter circuit

Fig. 4.3: Auxiliary chopping and switching circuits

level in this state so that the NBTI/PBTI (negative and positive bias temperature instability) effects which negatively affect the long-term reliability of the circuitry are minimized in power-down.

The stability of these opamps will be evaluated in the context of the feedback loops they control later on, some parameters of interest are nevertheless shown in Table 4.1. As the some of these parameters such as input common mode range (*ICMR*) and output common mode range (*OCMR*) are strongly dependent on V_{DD} and somewhat affected by temperature, the values shown are valid for PVT conditions as specified at the bottom of the table. The supply current of the opamp is considerable, but as was already mentioned, the opamp can be switched off to draw less than 1 nA even at 125 °C. The open loop gain narrowly meets the specification of 89 dB as was derived in subsection 3.2.4, though the closed loop gain of the overall feedback loops where the opamps are used is unfortunately usually smaller as will be shown later. It will however also be shown that this does not affect the overall error in any significant way.

The slew rate of the opamp is rather small as it is not important. Offset without chopping is around $1\,\mathrm{mV}/\sigma$, while after chopping it amounts to $3.6\,\mu\mathrm{V}/\sigma$, which is the residual charge injection and clock feedthrough induced error. The *CMRR* and *PSRR* are rather lackluster at higher frequencies, but as the DSP is capable of averaging out high frequency signals and noise, it should not matter. The only issue would be if the noise were to be correlated with the switching of the $\Sigma\Delta$ modulator or DSP itself, which could actually be nearly fatal for the sensor, as it cannot eliminate this type of noise. A special care should be therefore invested into ensuring that the switching noise of the digital circuits does not couple back into the analog front-end or the power supply itself. Separating power supply rails for analog and digital domains is normal practice, routing another power supply rail for

Tab. 4.1: Opamp performance

Quantity	Min	Mean/Typ.	Max	Std Dev
$I_{\text{opa supply}}$	—	7.7 µA	10 µA	—
DC Gain	88 dB	94 dB	107 dB	—
ICMR	0 V	—	2.2 V	—
OCMR	0.65 V	—	2.3 V	—
Slew rate	0.63 V µs^{-1}	0.81 V µs^{-1}	1.27 V µs^{-1}	—
Offset w/o chopping	−3.06 mV	55 µV	3.31 mV	1.07 mV
Offset with chopping	−12.7 µV	0.6 µV	11.4 µV	3.6 µV
CMRR (1 kHz)	110 dB	—	—	—
CMRR (1 MHz)	54 dB	—	—	—
PSRR (1 kHz)	91 dB	—	—	—
PSRR (1 MHz)	23 dB	—	—	—

Note: all values valid for $V_{\text{DD}} = 3$ V; *ICMR* and *OCMR* valid for 27 °C

the ΣΔ modulator which exists on the boundary of the domains is desirable as well.

The full schematics of the circuits including transistor sizing are in the appendices section. The opamp along with its biasing circuit and power-down switches is shown on Figure C.11 and Figure C.12 (the version with the level shifter), the input chopping switch is shown on Figure C.13 and the accurately clock-inverting chopping clock generator is shown on Figure C.5.

4.2.3 Biasing circuit design

The biasing circuit schematic diagram is shown on Figure 4.4 and the full schematic is shown on Figure C.2. The biasing current I_{bias} has been chosen to be 300 nA nominal at room temperature. This is based on Figure 2.1 – the ideal range of currents for the substrate bipolar device is approximately 50 nA to 10 µA. Because the biasing current has to be multiplied r times in the ΔV_{BE} generator, picking a value at the lower side of the range is preferable so that the multiplied current still resides in the ideal range. Choosing a lower value also results in lower power consumption, on the other hand the lower currents lead to rather large biasing resistor and larger error due to leakage at high temperatures. The area of the resistors can be decreased by decreasing m as lower values of m lead to smaller ΔV_{BE}, but lowering ΔV_{BE} makes the error caused by the mismatch of the opamp more significant in comparison. As both chopping and DEM will be implemented in the biasing circuit, choosing a relatively low value of m should not be a problem.

The following equation derived from (3.33) shows the calculation of R_{bias} where $m = 5$ was chosen and the typical value for β was taken from Figure 2.1.

$$\begin{aligned} R_{\text{bias}} &= \frac{\Delta V_{\text{BE}}}{I_{bias}} \cdot \frac{\beta+1}{\beta} = \frac{\frac{kT}{q} \cdot \ln m}{I_{bias}} \cdot \frac{\beta+1}{\beta} \\ &\approx \frac{\frac{k \cdot 300}{q} \cdot \ln 5}{300 \cdot 10^{-9}} \cdot \frac{2.5+1}{2.5} \approx 194\ \text{k}\Omega \end{aligned} \tag{4.1}$$

This value of R_{bias} is suitable for unsalicided P-doped high resistance polysilicon resistor. The resistance actual value was slightly altered to 200 kΩ based on simulation results for typical process corner.

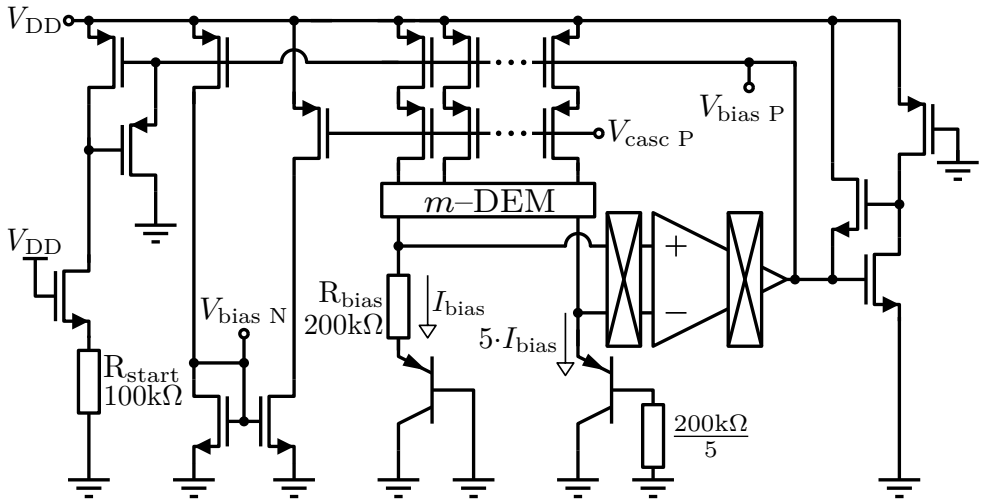


Fig. 4.4: Designed biasing circuit

As $m = 5$, there are 6 unit current sources which need to be dynamically matched to implement this ratio. Assuming $f_{\text{chop}} = 20\,\text{Hz}$, $f_{m\text{-DEM}}$ should be 12 times faster – 6 times for the 6 elements, and the additional multiplication by 2 ensures that the whole DEM cycle is completed twice during the chopping cycle, i.e. one full DEM cycle is completed during each chopping phase. Therefore, $f_{m\text{-DEM}} = 6 \cdot 2 \cdot 20\,\text{Hz} = 240\,\text{Hz}$.

The circuit on the right edge of the diagram on Figure 4.4 is basically identical to the start-up circuit with the transistors inverted (NMOS changed for PMOS and vice versa) and thus functions in exactly the opposite way. In some PVT corners, especially at the minimum temperature of −55 °C, the biasing circuit did end up in an operating point where the biasing current was too high and the opamp, which was biased by this current, did not have enough gain to regulate the biasing current. This circuit on the right side therefore serves as an "anti-startup circuit" – if the biasing current becomes too large, this circuit serves to lower it so that a stable operating point is found. Its sizing is relatively non-trivial, as it can in principle

"fight" the startup circuit – if this were to happen, the biasing circuit would produce wrong current.

The performance of this circuit is shown in Table 4.2. It can be seen that the offset voltage at the inputs of the opamp is $17\,\mu V/\sigma$. This is not the residual offset of the chopping method but rather a systematic error, which is caused by low gain in some PVT corners. The low gain is not primarily caused by the opamp itself but rather by the loop gain attenuation, which is in turn caused by the low g_m of the m-implementing current mirrors and their low impedance loads consisting of R_{bias} and the bipolar transistor's emitter impedance. The overall loop gain can therefore fall as low as 76 dB as seen on Table 4.2. This is essentially an inevitable property of this structure, but the error contribution of the overall offset is still negligible and should be only slightly larger than $\pm 0.01\,°C$ at 3σ (this was discussed in subsection 3.1.2).

The supply voltage sensitivity of the biasing circuit is extremely low and the m-ratio mismatch has been practically eliminated with DEM. The stability analysis graph is shown on Figure B.1 in the appendix.

Tab. 4.2: Biasing circuit performance

Quantity	Min	Mean/Typ.	Max	Std Dev
I_{bias} (27 °C)	257 nA	299 nA	340 nA	16.2 nA
Opamp offset	−81.5 µV	−7.6 µV	12.7 µV	17 µV
m	4.9999	5	5.00001	0.0006%
$S_{V_{DD}}^{I_{bias}}$	—	—	0.005 %/V	—
DC Loop gain	76 dB	87.2 dB	92.6 dB	1.9 dB
Phase Margin	74.9°	76.4°	77.4°	0.4°
Gain Margin	16.9 dB	17.6 dB	18.3 dB	0.3 dB
GBW	127.6 kHz	175.9 kHz	237.9 kHz	21.5 kHz

4.2.4 PTAT generator design

The schematic diagram of this circuit is depicted on Figure 4.5, the full schematic is shown on Figure C.6 and the stability analysis graph is depicted on Figure B.3.

As $r = 9$, there are 10 individual unit current sources which need to be dynamically matched. To ensure that the unit currents do not change during the r-DEM cycle, the cycle has to be 10 times faster than the m-DEM cycle. Therefore, $f_{r\text{-DEM}} = 10 \cdot 240\,Hz = 2400\,Hz$.

The resistance value of the V-to-I converting resistor has been chosen to be $100\,k\Omega$ as a compromise between area and power consumption.

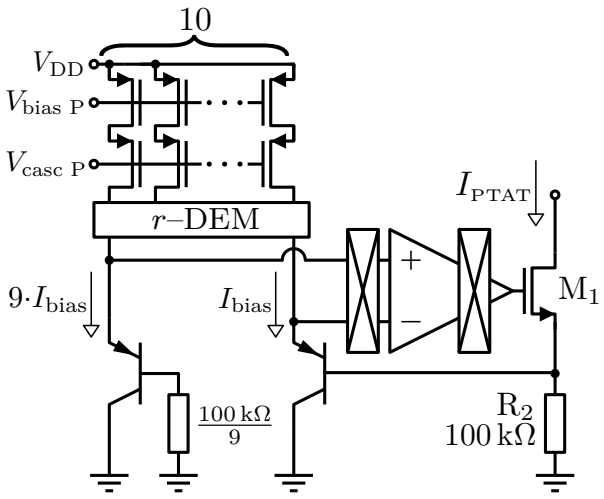


Fig. 4.5: Designed PTAT generator circuit

Tab. 4.3: PTAT generator performance

Quantity	Min	Mean/Typ.	Max	Std Dev
ΔV_{BE} (−55 °C)	41.5 mV	41.7 mV	41.9 mV	57 µV
ΔV_{BE} (125 °C)	75.1 mV	75.4 mV	75.6 mV	94.9 µV
Opamp offset	−39.9 µV	1.9 µV	39.8 µV	8.6 µV
r	8.9987	8.9990	8.9993	0.004%
DC Loop gain	74.8 dB	81.2 dB	89.1 dB	2.4 dB
Phase Margin	69.8°	73.4°	75.5°	0.8°
Gain Margin	38.9 dB	42.1 dB	44.9 dB	0.8 dB
GBW	297 kHz	379 kHz	490 kHz	37.5 kHz

As Table 4.3 shows, there is a significant spread associated with ΔV_{BE} which causes up to 0.2 °C/σ of measurement error. As m is quite precise due to DEM and the opamp offset is nearly negligible in comparison, this error cannot be explained by any of these external error sources. This spread is rather caused by the BJT devices themselves, namely their mismatch and their process spread. While ΔV_{BE} is largely process insensitive as shown in subsection 2.1.1, this insensitivity has its limits as this simulation shows. As the PDK of the TSMC 110 allows the designer to turn off the mismatch simulation of the BJT devices, it has been found out that the simulated spread of ΔV_{BE} with process and mismatch spread is about 95 µV/σ, while without mismatch, the process related spread is around 65 µV/σ (at 125 °C). Assuming both these errors are normally distributed and uncorrelated, the mismatch

contribution can be calculated as follows.

$$\sigma_{mis} = \sqrt{\sigma^2_{mis+proc} - \sigma^2_{proc}} = \sqrt{(95\,\mu\text{V})^2 - (65\,\mu\text{V})^2} \approx 70\,\mu\text{V} \tag{4.2}$$

This shows that the mismatch contribution to the spread of ΔV_{BE} is comparable to the process contribution. This is important because while the mismatch of the BJT devices is in principle removable by DEM, the process spread would have to be trimmed out (output trim as described in subsection 3.3.4 might help, but due to excessively long simulation time it has not been verified). This shows that employing DEM for the BJT devices in the PTAT generator would not bring significant improvement and the increased design complexity would probably not be worth it.

This error obviously also affects the biasing circuit which generates ΔV_{BE} voltage as well, but the ΔV_{BE} spread in the biasing circuit manifests as an increased spread in the biasing current which is trimmed anyway. Even without trimming, the overall measurement error caused by ΔV_{BE} spread in the biasing circuit is around ten times smaller in magnitude because V_{BE} is around ten times less sensitive, so it is only the PTAT generator which is severely affected by the ΔV_{BE} spread.

Lastly, the substrate leakage of the current regulating transistor M_1 is a source of both systematic and random error. This leakage current itself grows steeply with temperature (it can be usually ignored at temperatures lower than about 80 °C) and it is strongly dependent on process dependent parameters of the M_1 device. The leakage current flowing to the substrate from the drain of M_1 to its bulk is around 190 pA worst case, about one fourth of which is random. At 125 °C, the current I_{PTAT} is around 700 nA, which is about three orders of magnitude larger than the associated leakage. Nevertheless, the random spread of leakage can explain up to ±0.03 °C reading error at the top of the range as calculated by (2.19). Higher I_{PTAT} would solve this by increasing the "signal-to-leakage" ratio, but it would increase the power consumption as well.

4.2.5 Trimming circuit design

The trimming circuit is a part of the CTAT generator circuit but its design is non-trivial and thus it deserves its own section.

The trimming circuit should be able to compensate for the process spread of both the sensing BJT and the biasing current. Therefore, the worst corner cases are when the biasing current is low and the BJT is "fast", i.e. requires more current than typical to produce the V_{BE} voltage, and vice versa when the biasing current is high and the BJT is "slow", i.e. when it produces more V_{BE} than typical for given current. The trimming circuit has to be designed to ensure that it is capable of compensating both the possible worst case corners.

The spread of the biasing current is shown on Table 4.2 – its 3σ spread at room temperature is 257 nA to 340 nA. The spread of the BJT is known as well, though for the purpose of designing the trimming circuit, its more useful to quantify it in terms of current required to produce the modus value of V_{BE} (as it is the modus value which will be the trimming target). It has been simulated that at room temperature, the 3σ range of the biasing currents required to produce the modus value of V_{BE} is 230 nA to 360 nA.

These numbers can be used to determine the trimming circuit requirements. The first worst case is when the biasing current is low 257 nA and the BJT device needs 360 nA to produce the modus V_{BE} – multiplying the biasing current by 1.4 is necessary. In the opposite case, multiplication of the biasing current by a factor of 0.68 is needed. Therefore, assuming the typical value of the biasing current at room temperature is 300 nA, the trimming circuit should be able to control the current entering the bipolar device (denoted by I_{sense} as it flows into the sensing BJT) from $0.68 \cdot 300\,\mathrm{nA} = 204\,\mathrm{nA}$ typical to $1.4 \cdot 300\,\mathrm{nA} = 420\,\mathrm{nA}$ typical. This means that the 204 nA can be flowing into the BJT device at all times and only the rest of the current range should be controlled by trimming. The remaining 216 nA current range should be divided into binary weighted parts according to the required trimming precision. The following equations can be used to determine the necessary V_{BE} step, which can be further used to calculate the step of I_{sense} and therefore the total number of steps necessary.

$$V_{\mathrm{BE}}\ \mathrm{step} < 2 \cdot \frac{\varepsilon(\vartheta_{\mathrm{out}})}{S_{V_{\mathrm{BE}}}^{\vartheta_{\mathrm{out}}}} = 2 \cdot \frac{\varepsilon(\vartheta_{\mathrm{out}}) \cdot V_{\mathrm{REF}}}{T} \tag{4.3}$$

The V_{BE} step can be two times larger than the allowed V_{BE} error as the distance from the desired V_{BE} value to values accessible by trimming is always at most only one half of the step.

$$I_{\mathrm{sense}}\ \mathrm{step} < I_{\mathrm{bias}}\left[\exp\left(\frac{V_{\mathrm{BE}}\ \mathrm{step}}{V_{\mathrm{T}}}\right) - 1\right] \tag{4.4}$$

$$N_{\mathrm{step}} = \frac{I_{\mathrm{sense}}\ \mathrm{range}}{I_{\mathrm{sense}}\ \mathrm{step}} \tag{4.5}$$

If ±0.01 °C residual error at the trimming temperature is desired, the number of steps required is about 232, assuming room temperature trim. Using 8 bit trimming resolution seems quite excessive considering there are untrimmable errors in the circuit which amount to much greater errors than ±0.01 °C, such as the processing spread of ΔV_{BE}. Targeting residual error of ±0.1 °C leads to 23 steps or 5 bits, which is more reasonable.

In this design, 6 bit trimming resolution has been chosen because it has been found out that the precision of PTAT trimming of V_{BE} is severely affected by its

residual curvature, which is roughly halved but not completely removed by using strongly PTAT biasing current. Because the curvature of V_{BE} is a non-linear error, PTAT trimming is incapable of removing it at any other temperature than the trimming temperature. Similarly to the situation outlined at the end of subsection 3.3.4,

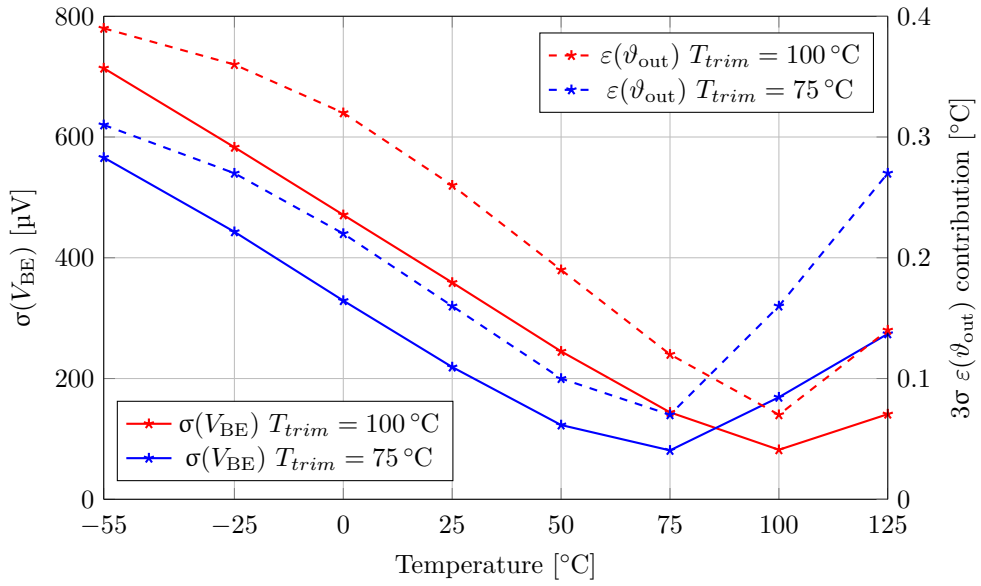


Fig. 4.6: Residual V_{BE} spread after trimming and its equivalent reading error

the residual spread of V_{BE} caused by this curvature is increasing towards the edges of the temperature range. Including the additional bit of resolution helped to slightly reduce this effect. Nevertheless, this residual curvature induced error amounts to up to $\pm 0.3\,^{\circ}\mathrm{C}$ of error and further improvement is only possible with full-fledged curvature correcting circuitry implemented in the analog domain.

To achieve the same error contribution of the residual V_{BE} spread on both ends of the temperature range, the residual spread at $125\,^{\circ}\mathrm{C}$ should be about half as large as the spread at $-55\,^{\circ}\mathrm{C}$, because the sensitivity of the measurement to the errors in V_{BE} is PTAT as (2.15) shows. This would mean that the ideal trimming temperature is somewhere close to two thirds of the temperature range, which is $65\,^{\circ}\mathrm{C}$. However, because the are other errors in the circuit, it may be beneficial to choose a different trimming temperature. For example, if a large PTAT random error remains in the circuit, it may be better to compensate for this by further reducing the remanent V_{BE} error at the top of the temperature range by choosing a trimming temperature closer to $125\,^{\circ}\mathrm{C}$. This is precisely the case for this design as will be shown later. Therefore, the trimming temperature was chosen to be $100\,^{\circ}\mathrm{C}$. The effect of $\vartheta_{\mathrm{trim}}$ on the measurement error is shown on Figure 4.6.

It is important to note, however, that the trimming temperature is not something the designer can usually control, especially if the sensor is designed as an IP core.

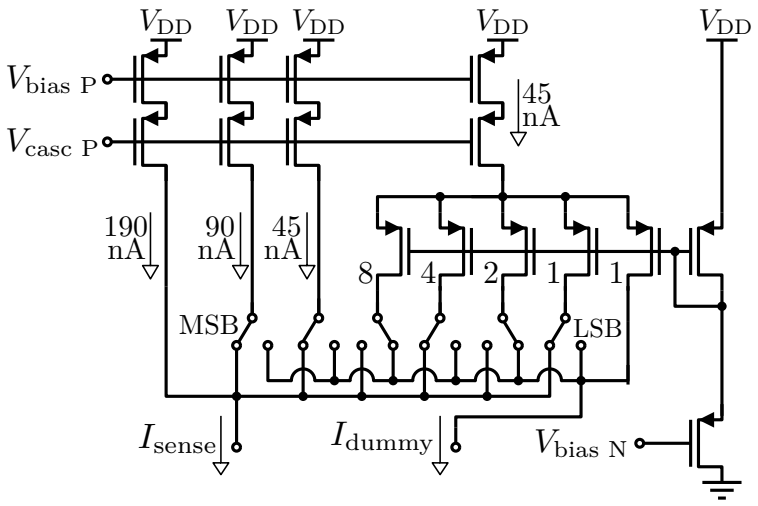


Fig. 4.7: Current trimming circuit with 6 bit resolution

The IP core is often directly ordered by the customer for his own chip, which might include other circuits, some of which might need trimming as well. In that case, the trimming temperature is specified by the customer beforehand. If the IP core is designed as an "off-the-shelf" product, the designer can at most recommend the optimal trimming temperature in the IP core implementation guide. And finally, even if the sensor is to be manufactured as a standalone chip, the choice of the trimming temperature might be simply economical – the closer the trimming temperature is to the edges of the range, the higher the demands for the necessary trimming equipment and the more time it takes for the chips to settle at this temperature, which is a logistical issue during the production.

The designed trimming circuit is shown on Figure 4.7. The current dividing cascodes (which are made of binary multiples of unit elements, as shown on the

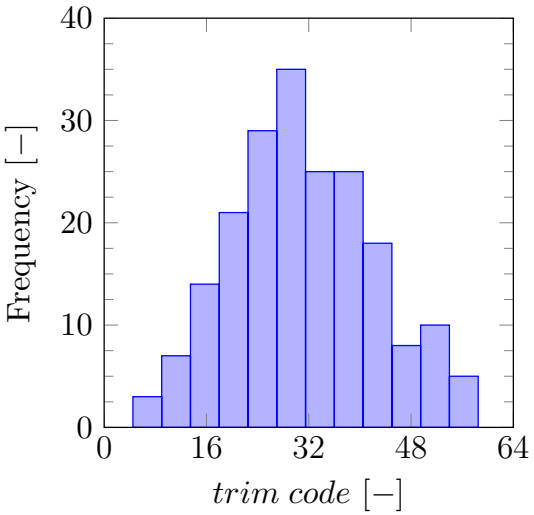


Fig. 4.8: Trimming code histogram

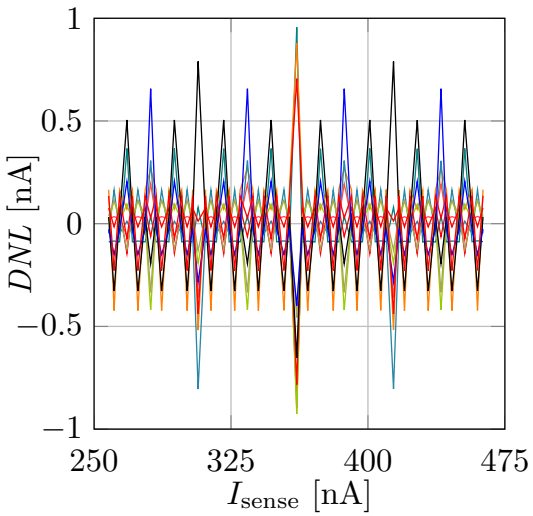


Fig. 4.9: Trimming circuit *DNL*

full schematic on Figure C.7) are biased by the voltage $V_{\text{bias N}}$ which is generated in the biasing circuit which is depicted on Figure 4.4. The calculated currents (shown values correspond to room temperature) have been slightly altered to ensure that 3σ yield of chips (97.5%) fit the trimming range as seen on Figure 4.8. At the trimming temperature $\vartheta_{\text{trim}} = 100\,°\text{C}$, the ideal step of I_{sense} is about 3.3 nA. Therefore the *DNL* of the trimming circuit, the most important parameter characterizing its precision, is at worst still less than $\frac{1}{3}$ of *LSB*, as evidenced by several worst case runs from Monte Carlo simulation shown on Figure 4.9.

The method of simulating trimming is described in the appendix chapter A as it deserves more attention.

4.2.6 CTAT generator design

The CTAT generator circuit is depicted on Figure 4.10. Similarly to the PTAT generator its design is straightforward. The resistance value is 100 kΩ just as the resistor in the PTAT generator so that these resistors can be matched in layout.

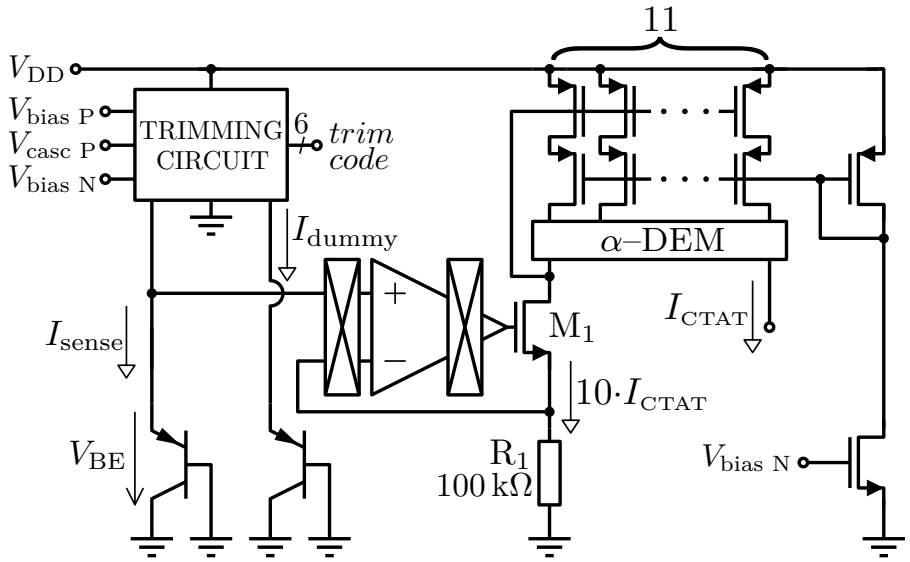


Fig. 4.10: Designed CTAT generator circuit

The stability analysis graph is shown on Figure B.2 in the appendix.

Substrate leakage at high temperature is a potential issue. The leakage in this circuit comprises of several parts. Each transistor of the α-mirror can leak up to 350 pA, and the current regulating transistor M_1 leaks up to 230 pA. About one fourth of the mentioned worst case values is random. As ten of the α-mirror transistors are connected to the current regulating transistor M_1 and only one of the α-mirror current sources is connected to the output node, it is difficult to evaluate the overall effect on the measurement. The simplest estimate can be calculated with

Tab. 4.4: CTAT generator performance after trimmming

Quantity	Min	Mean/Typ.	Max	Std Dev
V_{BE} (−55 °C)	800.5 mV	802.5 mV	804.3 mV	714 µV
V_{BE} (25 °C)	695.4 mV	696.7 mV	746.3 mV	471 µV
V_{BE} (100 °C)	504.8 mV	505.0 mV	505.2 mV	82 µV
V_{BE} (125 °C)	456.8 mV	457.1 mV	457.5 mV	141 µV
Opamp offset	−62.2 µV	−1.3 µV	50.4 µV	15.1 µV
α	9.998	10.000	10.010	0.012%
DC Loop gain	78.9 dB	91.3 dB	102 dB	2.6 dB
Phase Margin	72.1°	75.1°	78.9°	1°
Gain Margin	34.2 dB	36.9 dB	39.7 dB	0.5 dB
GBW	687 kHz	958 kHz	1.33 MHz	125 kHz

(2.20) assuming only the leakage current flowing into the output node matters. This leads to 3σ random measurement error ±0.05 °C at 125 °C.

4.2.7 Resistor DEM controller design

During the design it has been decided that employing DEM for the V-to-I converting resistors is desirable. This is because it has been found that 2 µm wide resistors (which is a width few times larger the minimum width already) match to about 0.1%/σ. This mismatch directly translates to an error in α. Assuming 3σ yield, 0.3% error in α causes up to ±0.5 °C temperature reading error.

While the m, r and α DEM controllers are very simple blocks featuring only minimum size switches and inverters (as seen on their schematic diagrams Figure C.10, Figure C.8 and Figure C.9), the resistor DEM controller needs more careful approach because the switches inside are not in series with current sources and their R_{DSon} is therefore not negligible.

So-called Kelvin connection can be adopted to minimize the switch area. The Kelvin connection utilizes two "lines" – the force line and the sensing line. The force line forces a current, while the sensing line leads to a high impedance sensing input (for example an input terminal of an opamp) and thus passes no current. This can be seen on the left side of Figure 4.11, which depicts a part of the CTAT generator circuit – in the state which is shown, the force line forces a current through the force switch F_1 which flows into the resistor below, while the connection realized by the switch S_1 closes the feedback loop at the resistor's terminal. Even though there is a significant voltage drop across minimum sized switch F_1, the sensed node

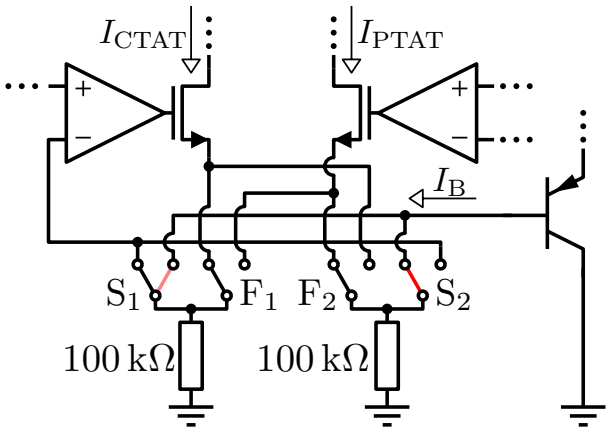


Fig. 4.11: Designed resistor DEM controller with wide switches highlighted in red

is below the switch and the voltage drop of F_1 is "accounted for" by the feedback loop. As there is no voltage drop across the minimum sized S_1 either (it passes no DC current), the feedback loop functions perfectly.

A problem arises with the PTAT generator, a part of which is shown on the right side of Figure 4.11. This is because its sense line – the wire connecting the resistor to the base of the bipolar transistor – actually passes a non-negligible current as well, namely the base current I_{B} of the bipolar transistor. This means that the switch S_2 cannot be minimum size and should be instead rather wide so that the voltage drop across it is minimal. This is an unfortunate property of this type of PTAT generator and a completely different architecture would have to be chosen to ensure that all the switches can be minimum size. However, the area price is not that severe – to ensure the voltage drop is on the level of few µV at most, the larger switch has been designed to consist of three parallel 20×0.385 µm NMOS transistors. While this is about 400 times larger than the minimum size switch, it is still roughly 16 times smaller than one bipolar device, of which there are six instances in the design. More problematic is the leakage associated with the wide switch, which is not negligible at few hundred pico Amperes and causes a semi-random, semi-systematic error.

Because this is a DEM controller, all the switches can be set to one of two possible positions so that the resistors can be interchanged. This means that in one phase, F_1 and S_1 force and sense CTAT signals, while in the other phase they force and sense PTAT signals and vice versa for F_2 and S_2. Therefore, there are actually two problematic switches which have to be made large due to the PTAT generator's bipolar transistor base current, and on Figure 4.11, they are shown in red. The full schematic of this controller is shown on Figure C.4 in the appendices section.

Because the α–DEM controller inputs a current which changes based on the R–DEM cycle, α–DEM controller has to be the fastest running DEM cycle in the design. The resistor matching R–DEM cycle can run at two times the speed of

the r–DEM controller, i.e. $f_{\text{R-DEM}} = 2 \cdot f_{r-\text{DEM}} = 2 \cdot 2400 = 4800\,\text{Hz}$. Therefore, $f_{\alpha\text{-DEM}} = 11 \cdot f_{\text{R-DEM}} = 11 \cdot 4800 = 52\,800\,\text{Hz}$. This is fairly high frequency and depending on the required oversampling ratio of the $\Sigma\Delta$ modulator, conversion period specifications etc. implementing dynamically matched resistors might not be worth the precision increase.

4.2.8 Layout considerations

The layout of the designed analog front-end is not the goal of this thesis, as design engineers are usually not qualified enough in this area. The designer however has to understand how the layout of his circuits can affect their performance and he should therefore include notes and guidelines for the layout engineers in the schematics so that suboptimal layout does not introduce any unnecessary and unwanted parasitics into these sensitive circuits.

The obvious and most important layout consideration is matching of identical elements. In this particular design, there are few devices which do not need to be matched to any other device. Differential pairs, current mirrors, cascodes, resistors and the bipolar devices are prime examples of critical subcircuits and elements which should be carefully matched by placing them in various interdigitized or symmetric configurations, ensuring temperature or doping gradients affect all devices evenly.

Biasing current mirrors require closer attention. Because their role is to distribute the currents to various, often quite distant parts of the analog front-end, it is the actual current and not the gate voltage which should be passed across these larger distances. This is because the gate voltage V_{GS} is usually referenced to ground or to the supply rail, both of which have current flowing through them, which can induce a voltage drop across the interconnect resistance. This situation is illustrated on Figure 4.12. If the two current mirror transistors are far apart, the distributed value of V_{GS} generated at the current mirror input may produce a different current at the current mirror output simply due to the fact that at the output transistor, the V_{GS} voltage has to include the interconnect voltage drop as well. In this example, the output current would be smaller than it should be. Keeping these transistors close and routing the output current of the output transistor across large distances instead is a better option.

Another technique which has to be used when laying out precision circuits are dummy devices. These unconnected devices surround the matched resistors, differential pairs, cascodes or current mirrors and ensure that the boundary conditions of the matched devices are symmetric. Even less known effects such as Shallow Trench Isolation stress or well proximity effects [27] should be taken into account.

Implementing ratios of elements (resistors or MOS transistors) should be always

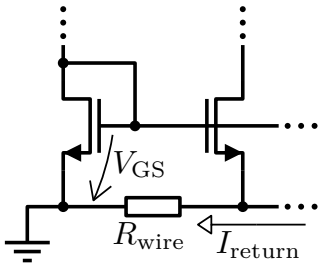


Fig. 4.12: Current mirror interconnect resistance

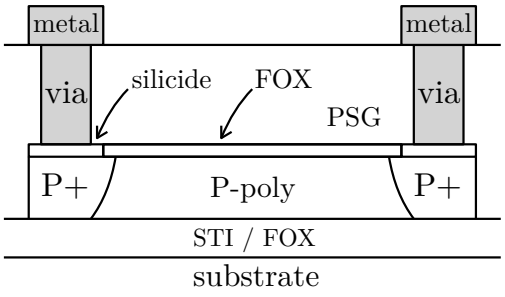


Fig. 4.13: Polysilicon resistor cross-section

done using multiples of parallel or series connected unit sized elements. This is especially important for resistors, because the polysilicon resistor is actually made up of two resistors – the body resistor, which is made from polysilicon, and the "head" resistor, which is a parasitic series resistor made up from the various contact resistances that exist at the boundaries of the metal layer, the via, the silicide layer, the P-doped silicon and finally the P-doped polysilicon, as seen on Figure 4.13. The "head" resistor has its own TCR which differs from the TCR of the body resistor. When implementing a certain ratio of resistances, this differing TCR may cause the overall resistance ratio to change with respect to temperature. The "head" resistor should therefore be ratioed as well, which is accomplished by implementing the smaller of the two ratioed resistors as a unit and the larger one as a series connection of integer amount of said units. This way, the proportion of the head resistor to the body resistor is the same for both the ratioed resistors and the overall resistance ratio should be temperature independent. Otherwise, this effect could introduce large errors to the biasing and the PTAT generator circuits, which utilize a ratio of two different sized resistors for β compensation.

Another important consideration is shielding. As the ADC is a high speed $\Sigma\Delta$ modulator and other high speed digital circuits are often included on the die, the analog front-end should be shielded from these high frequency switching signals so that they do not couple into critical signal paths and corrupt the measurement. Substrate noise isolating guard rings or grounded metal interconnects surrounding critical signal paths help to diminish this effect.

Lastly, the analog front-end includes several feedback loops whose stability may be affected by parasitic capacitances, running post-layout parasitic extraction and re-checking the stability of the loops is therefore advisable as well. Post-layout parasitic extraction may also reveal potential interconnect resistance issues.

The precision layout techniques take up additional area and some level of margin should be included in the estimation of the total area. Assuming 20% margin for routing, dummies etc. is included, which is a reasonable amount for carefully laid out precision circuits, the total area of the analog front-end would be $0.012\,\mathrm{mm}^2$.

4.3 Achieved performance

The ideal ADC and DSP equations (2.12) and (2.14) were used to convert the simulated analog quantities into temperature reading in Celsius, utilizing $A = 641.5\,°C$ and $B = -274.4\,°C$ (these values were found by mathematical interpolation of μ). The achieved performance of the circuit simulated over several hundreds of Monte Carlo runs is summarized in Table 4.5.

Tab. 4.5: Achieved performance

Quantity		Min	Mean/Typ.	Max	Std Dev
Area		—	$0.012\,mm^2$	—	—
V_{DD}		2.7 V	3 V	3.63 V	—
I_{DD} (active)		—	—	57 µA	—
I_{DD} (power down)		—	—	8 nA	—
Power consumption		—	10 µW	—	—
$S_{V_{DD}}^{\vartheta_{out}}$		—	—	$0.05\,°C\,V^{-1}$	—
$\varepsilon(\vartheta_{out})$ w/o DEM & chopping		−12.7 °C	0.66 °C	13.4 °C	3.92 °C
$\varepsilon(\vartheta_{out})$ untrimmed	−55 °C	−0.59 °C	0.24 °C	1.10 °C	0.39 °C
	−25 °C	−0.94 °C	0.05 °C	1.14 °C	0.49 °C
	0 °C	−1.27 °C	−0.08 °C	1.24 °C	0.58 °C
	25 °C	−1.61 °C	−0.18 °C	1.39 °C	0.69 °C
	50 °C	−1.93 °C	−0.23 °C	1.61 °C	0.82 °C
	75 °C	−2.22 °C	−0.23 °C	1.92 °C	0.95 °C
	100 °C	−2.47 °C	−0.15 °C	2.32 °C	1.09 °C
	125 °C	−2.67 °C	0.03 °C	2.82 °C	1.24 °C
$\varepsilon(\vartheta_{out})$ after trimming	−55 °C	−0.3 °C	0.13 °C	0.55 °C	0.17 °C
	−25 °C	−0.43 °C	0.01 °C	0.43 °C	0.17 °C
	0 °C	−0.52 °C	−0.07 °C	0.35 °C	0.16 °C
	25 °C	−0.58 °C	−0.13 °C	0.30 °C	0.16 °C
	50 °C	−0.60 °C	−0.15 °C	0.28 °C	0.16 °C
	75 °C	−0.57 °C	−0.12 °C	0.31 °C	0.17 °C
	100 °C	−0.49 °C	−0.03 °C	0.41 °C	0.18 °C
	125 °C	−0.38 °C	0.12 °C	0.60 °C	0.21 °C

The maximum allowed supply voltage is given by the technology, while the minimum supply voltage is limited by the CTAT circuit, where at low supply voltages the opamp cannot drive the gate of the current regulating transistor at its output high enough. Using a native transistor instead of normal one might solve this issue, but then at 2.5 V the biasing circuit would become the limiting factor.

The supply current during conversion is mostly given by the currents drawn by the three opamps. In power down mode, the supply current consists of leakage, which rises rapidly with temperature. At room temperature the power down current is on the order of few pA and the nA leakages appear only at the top of the temperature range.

These supply currents directly affect the average power consumption, just as the conversion time and the sample rate. The typical conversion time was chosen to be 50 ms back in subsection 4.2.1. The fastest DEM frequency in this design is 52.6 kHz. Assuming the ΣΔ modulator runs at several tens of MHz, increasing the speed of all the chopping and DEM circuits by a factor of 10 may still be feasible without sacrificing precision or insensibly increasing the demands for the ΣΔ modulator. This is because the ΣΔ modulator should run at significantly higher frequency than the signal it modulates to maximize the oversampling ratio and thus minimize the quantization noise. Assuming the sample rate is 1 measurement per second, 995 ms can be then spent in power down mode. On average, analog front-end power consumption of 0.1 µW to 10 µW at worst case temperature 125 °C can be expected depending on the sample rate and the conversion period.

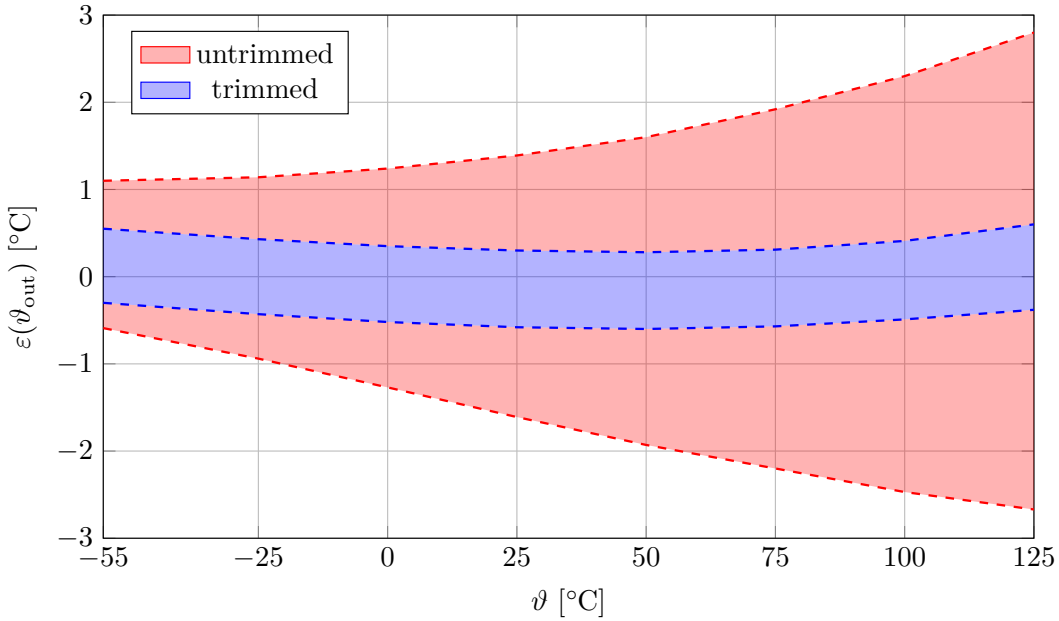


Fig. 4.14: Temperature dependence of measurement error

As for the precision of the circuits, the performance can be more clearly depicted on the following figures. As Figure 4.14 shows, the dominant error before trimming is PTAT, which is caused by the spread of the saturation current I_S and the spread of the resistor in the biasing circuit as was already discussed numerous times. After trimming, the remanent curvature of V_{BE} can be clearly seen as it amounts to about 0.3 °C non-linearity.

The histograms shown on Figure 4.15 and Figure 4.16 are not as useful as the chart on Figure 4.14, but they better show the actual statistical distribution of the error. It is important to note the histograms show the statistical distribution of the error across all PVT conditions, i.e. including temperature. This is why the shape of the histograms does not necessarily follow normal distribution.

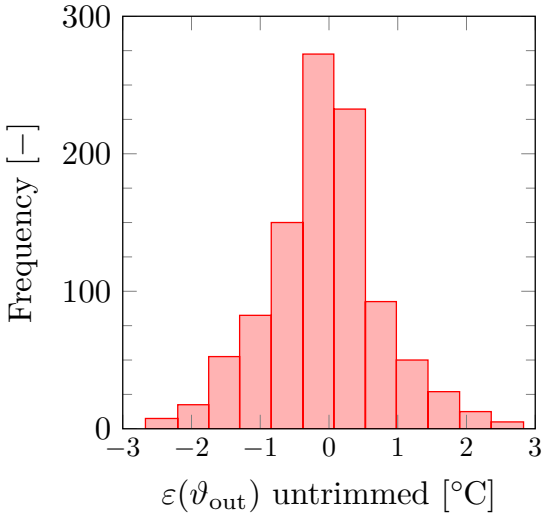


Fig. 4.15: Histogram of untrimmed error

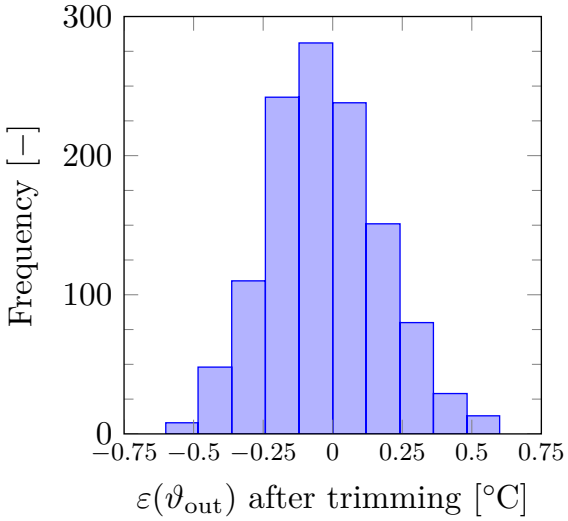


Fig. 4.16: Histogram of trimmed error

For comparison, the 3σ precision without DEM and chopping running is around ±12 °C, which shows how crucial their role is.

4.3.1 Residual error analysis

In this subsection, error contributions of various error sources will be analyzed and quantified. The summary is shown in Table 4.6.

This table should be understood as a rough error contribution calculation. There are some errors which have been ignored, and some of the included errors, especially the ones originating in the biasing circuit, are "trimmed out" in the CTAT generator, which changes their overall effect on the measurement in a complex manner. Some errors are also "included twice" – for example a spread in r manifests as a spread of ΔV_{BE}, which is shown as well, though it might be interesting to see how much of the total measurement error can be solely accounted to the individual parts such as r spread.

Tab. 4.6: Random residual errors after trimming and their temperature reading error contribution

Error source	3σ error signal deviation			Affected signal	Equivalent 3σ $\varepsilon(\vartheta_{\text{out}})$ deviation		
	−55 °C	50 °C	125 °C		−55 °C	50 °C	125 °C
Bias ΔV_{BE}*	141 µV	193 µV	262 µV	V_{BE}	0.03 °C	0.05 °C	0.08 °C
Bias opamp offset*	51.9 µV	44.1 µV	37.5 µV	V_{BE}	0.006 °C	0.007 °C	0.008 °C
m*	0.002%	0.001%	0.001%	V_{BE}	$<10^{-3}$ °C	$<10^{-3}$ °C	$<10^{-3}$ °C
V_{BE}	2.1 mV	757 µV	424 µV	V_{BE}	0.39 °C	0.19 °C	0.14 °C
Current mirror α	0.012%	0.003%	0.002%	α	0.02 °C	0.005 °C	0.003 °C
CTAT opamp offset	52 µV	41 µV	34 µV	V_{BE}	0.01 °C	0.01 °C	0.01 °C
ΔV_{BE}	165 µV	219 µV	285 µV	ΔV_{BE}	0.58 °C	0.58 °C	0.57 °C
r	0.002%	0.002%	0.004%	ΔV_{BE}	0.001 °C	0.001 °C	0.003 °C
Resistor ratio α	0.016%	0.015%	0.03%	α	0.02 °C	0.02 °C	0.05 °C
PTAT opamp offset	24.6 µV	20.7 µV	19.2 µV	ΔV_{BE}	0.09 °C	0.05 °C	0.04 °C
Leakage currents	—	—	200 pA	I_{CTAT}, I_{PTAT}	—	—	0.07 °C
Total 3σ error					0.51 °C	0.56 °C	0.64 °C

* affected by trimming

Tab. 4.7: Correlation of V_{BE} and ΔV_{BE} induced temperature reading error

Temperature	−55 °C	50 °C	125 °C
$\rho(V_{\text{BE}} - \Delta V_{\text{BE}})$	–0.55	–0.3	0.45

The leakage current errors were combined as if they were uncorrelated, which is obviously not realistic, but the table serves just as an estimation. Their value at lower temperatures is negligible and even at 125 °C the error contribution is small.

Utilizing Cadence Virtuoso scatter plot functionality, it has been found that the temperature errors caused by the spread of V_{BE} and ΔV_{BE} are correlated (which is not surprising, as both errors are caused by the same device). The correlation means that the total error spread cannot be calculated with the following equation

$$\sigma_{total} = \sqrt{\sigma_1^2 + \sigma_2^2} \tag{4.6}$$

but rather its full form has to be used

$$\sigma_{total} = \sqrt{\sigma_1^2 + \sigma_2^2 + 2\rho\sigma_1\sigma_2} \tag{4.7}$$

where ρ is the correlation of the two random variables [28].

The correlation factor of the V_{BE} and ΔV_{BE} induced errors varies with temperature and is shown on Table 4.7. The correlation is negative at temperatures below the trimming temperature, which means that the errors tend to cancel out, while above the trimming temperature, they tend to add and further increase the total error. This is the reason for why high trimming temperature was chosen back in subsection 4.2.5. It is highly likely some other errors correlate too, but their magnitude is quite small for the correlation to matter significantly.

The total resulting error calculated from the individual contributions decently matches the simulated results shown in Table 4.5 which means that all important errors were accounted for and the magnitude of the individual error contributions was estimated at least somewhat correctly.

It is obvious that the most dominant error is the spread of ΔV_{BE}. As was shown in subsection 4.2.4, this error stems from both mismatch and process contributions which are roughly the same in magnitude. This means that this error cannot be significantly improved by DEM of the bipolar transistors and additional trimming circuits would be necessary. If this error were to be removed, the residual error of V_{BE} caused by remanent curvature would become the limiting factor. The only ways to remove this error would be to either trim at multiple temperatures (which is usually impossible due to economical reasons) or to include analog curvature correction circuitry. This circuitry tends to be rather complex and area intensive as it often requires its own bandgap reference and as such it is also subject to random errors, therefore the curvature correcting circuitry would require trimming of its own. If this error were to be be removed as well, only then would the small errors such as charge injection caused mismatch of dynamically matched elements and chopped opamps, insufficient loop gains or leakage currents at high temperature become dominant.

4.3.2 Comparison with the state of the art

In this subsection, the achieved results of this art will be compared to the current state of the published art.

Comparing the achieved results with published art is not a simple task. First of all, in this thesis, only the analog front-end was designed, while published art includes the ADC and DSP circuits as well. These circuits take up extra area and may cause additional error, though usually it is the analog front-end which limits the precision and the ADC with the DSP tend to contribute much less to the overall measurement error. Secondly, the designed sensors should always be compared with the desired specifications – in some applications, energy efficiency is the highest priority. In others, it may be the area, the sample rate, the number of trims etc.

Assuming precision and area are our figures of merit, a chart showing the relationship between the area and precision of published sensors can be constructed. This chart is based on a survey of smart temperature sensors papers published between 1989 and the present and which is managed by the Precision Analog Group at the Delft University of Technology [29]. The sensors marked by the crosses are all BJT-based and their errors are measured after single trimming operation.

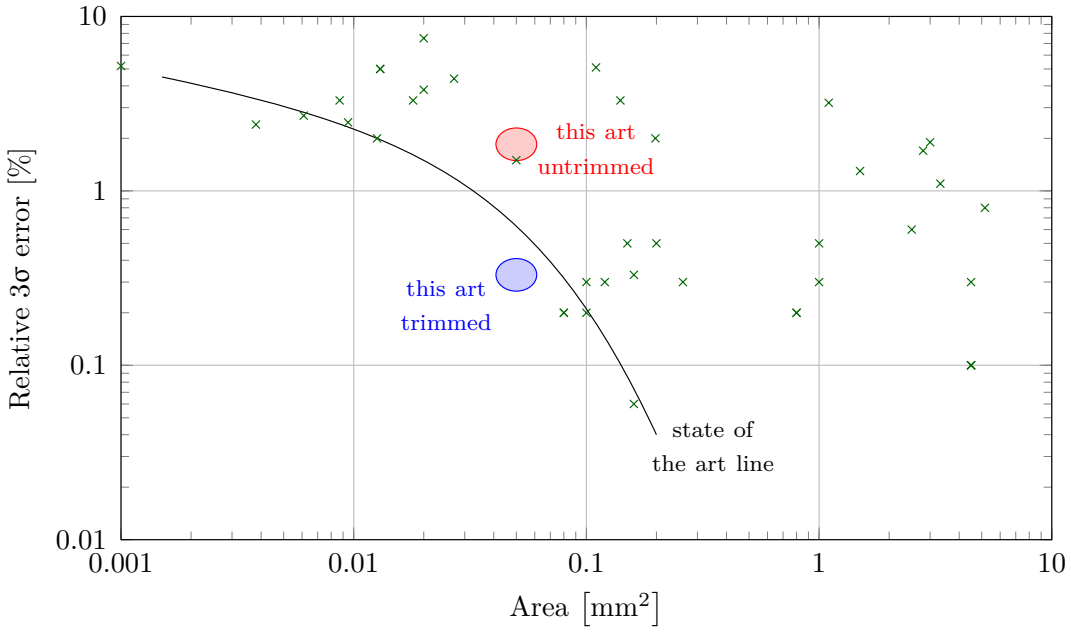


Fig. 4.17: Area vs. relative error chart of published sensors including this art

The Y-axis of the chart shows the "relative error" for 3σ yield, which is a ratio of the maximum 3σ measurement error and the sensor's temperature range

$$\text{Relative error} = \frac{\varepsilon(\vartheta_{\text{out}})}{\vartheta_{\text{max}} - \vartheta_{\text{min}}} \cdot 100\% \tag{4.8}$$

The 3σ relative error of this art is about 1.7% untrimmed or 0.33% trimmed.

In order to place the sensor designed in this art on the chart, the area including the ADC and the DSP has to be estimated. Based on sensors which have been designed in similar process nodes (both several published sensors and mainly one unpublished one which the author has access to), it has been concluded that the total area would probably lie in the 0.04 to 0.06 mm^2 range.

This art can be then placed on the chart and it is denoted by the red and blue ellipses, the red one for the case when it is left untrimmed and the blue one for the case when proper trimming has been performed on each chip. Additionally, a line approximately connecting the best sensors published to this date has been constructed and denoted "state of the art line". The sensor designed in this thesis lies in the proximity of the line after trimming, which proves that this design is competitive with the current state of the published art. This sensor also lies close to the middle of the line, which means that this design strikes a good balance between area and precision, which was the main goal of this design as mentioned in subsection 4.2.1.

Obviously, the other published art on the chart has been manufactured and the data is therefore based on real and not only simulated results. There is also the fact that the TSMC 110 PDK does not model some effects such as the spread of TCR, which may have negative effect on the accuracy, along with packaging stress etc.

However, it has to be repeated that the published art is mostly academic in origin and very few samples have been actually manufactured and measured (usually less than 30), most of which come from a handful of wafers at most, and those wafers usually come from the same processing batch. Their measurements have been therefore done on a handful of chips which were most likely all similar to each other process variation wise. Therefore, if the chips were to be manufactured in mass volume over several months or years, the inaccuracy of the sensors would probably spread more than the published results suggest.

As the Monte Carlo simulation used in this thesis tries to simulate the effect of real process variation, in a sense the results of the simulations may predict the accuracy of the sensors better than the actual manufactured samples of the previously published art. While this art would probably achieve worse accuracy than the simulations suggest due to effects which are not modeled in the model files and due to additional error caused by the ADC and the DSP, the published art is probably worse then reported as well.

To close this subsection, it should be noted that industrial specifications for smart temperature sensor IP cores are usually measured for 4σ yields due to economical aspects, and the desired accuracy in common temperature monitoring applications is usually around $\pm 2\,^{\circ}\mathrm{C}$ at 4σ, which this art satisfies with a large margin.

5 SUMMARY

In chapter 1, the main four possible ways of implementing a smart temperature sensor in standard CMOS process technologies were presented and compared according to their advantages and disadvantages. It was concluded that the bipolar transistor method is well-rounded and optimal for most general applications, and this method was further explained in chapter 2, where the necessary bipolar device physics, system level overview or mathematical error sensitivity analysis were discussed.

In chapter 3, circuit solutions and techniques used to implement precise BJT-based smart temperature sensor analog front-ends such as chopping or DEM were presented and the associated errors were quantitatively analyzed. The actual design of the analog front-end of a bipolar transistor based smart temperature sensor in TSMC 110 CMOS processing technology has been described in chapter 4. Techniques such as chopping, DEM, ratiometric curvature correction or β compensation were used to achieve high precision, power-down circuits and a trimming circuit were designed as well, and important considerations for laying out the analog front-end were briefly outlined.

According to computer simulation, the achieved precision is about $\pm 3.5\,^{\circ}\mathrm{C}$ untrimmed and $\pm 0.6\,^{\circ}\mathrm{C}$ after a single point trim at 3σ yield. The area of the analog front-end has been estimated to $0.012\,\mathrm{mm}^2$. Residual sources of error were presented towards the end of chapter 4, where it has been shown that removing the remaining dominant errors would require disproportionately complex additional circuitry, more trimming operations or a completely new architecture. Finally, comparison with the best sensors published to this date was presented, proving that the analog front-end presented in this thesis is competitive with the current state of the art and strikes a good balance between precision and area, which was the main goal of the design.

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LIST OF SYMBOLS, PHYSICAL CONSTANTS AND ABBREVIATIONS

ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuits
BJT	Bipolar Junction Transistor
CTAT	Complementary To Absolute Temperature
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DC	Direct Current
DEM	Dynamic Element Matching
DSP	Digital Signal Processing
DTMOS	Dynamic Threshold MOS
ETF	Electrothermal Filters
FOX	Field Oxide
FLL	Frequency Locked Loop
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
IP	Intellectual Property
LSB	Least Significant Bit
MEMS	Micro-Electro-Mechanical System
MIM	Metal-Insulator-Metal
MOS	Metal Oxide Semiconductor
MOM	Metal-Oxide-Metal
MSB	Most Significant Bit
NBTI	Negative Bias Temperature Instability
NMOS	N-channel MOS
opamp	operational amplifier
PBTI	Positive Bias Temperature Instability
PDK	Process Design Kit
PDM	Pulse Density Modulation
PMOS	P-channel MOS
PSG	Phosphosilicate Glass
PTAT	Proportional To Absolute Temperature
PVT	Process-Voltage-Temperature
RDF	Random Dopant Fluctuation
RFID	Radio Frequency Identification
RTC	Real Time Clock
SoC	System on Chip

SOI	Silicon on Insulator
STI	Shallow Trench Isolation
TI	Temperature Independent
V-to-I	Voltage to Current

α	PTAT signal scaling factor
A	gain factor used in the DSP temperature reading conversion
A_{E}	bipolar transistor emitter size
A_{OL}	opamp open loop gain
β	BJT current gain
B	offset factor used in the DSP temperature reading conversion
C	capacitance
$CMRR$	common mode rejection ratio
δ	relative error
D	thermal diffusivity
D_{p}	hole diffusion constant
DNL	differential non-linearity
ε	absolute error
GBW	gain-bandwidth product
g_{m}	mutual transconductance
I_{B}	base current
I_{C}	collector current
I_{DD}	supply current
I_{E}	emitter current
I_{S}	saturation current
$ICMR$	input common mode range
k	Boltzmann constant
μ	charge carrier mobility
m	biasing circuit current ratio
N_{D}	donor concentration
n	number of bits in a digital bus
n_{i}	intrinsic carrier concentration
$OCMR$	output common mode range
$PSRR$	power supply rejection ratio
ρ	Pearson's correlation coefficient
R	resistance
r	ΔV_{BE} generator current ratio

σ	standard deviation
S_{in}^{out}	sensitivity of the output quantity to changes in the input quantity
SNR	signal-to-noise ratio
TCR	temperature coefficient of resistance
t_{ox}	gate oxide thickness
q	elementary charge
T	thermodynamic temperature [K]
ϑ	temperature [°C]
ϑ_{out}	output temperature reading
$\vartheta_{\mathrm{trim}}$	trimming temperature
V_{BE}	base-emitter voltage
V_{GS}	gate-source voltage
V_{g0}	band gap voltage of silicon for T=0 K
V_{DS}	drain-source voltage
V_{DD}	supply voltage
V_{T}	thermal voltage
V_{th}	threshold voltage
W_{B}	bipolar transistor base region width

LIST OF APPENDICES

A SIMULATING TRIMMING IN CADENCE VIRTUOSO ADE

Simulating trimming in Cadence Virtuoso Analog Design Environment is a complex problem that is worth describing in closer detail. Essentially, two subsequent simulations have to be done – one to determine the proper trimming code, and the second one to analyze the temperature dependence of the temperature reading error taking the proper trimming code determined previously as an input. These two simulation tests will be called `untrimmed` and `trimmed`.

In the `untrimmed` test, the trimming code has to be determined. The most obvious way of doing this is by sweeping the trimming code at some given trimming temperature and looking at some variable of interest, which should preferably be equal to some ideal value. In this case it is the median value of V_{BE} at the trimming temperature. The value of trimming code which is desired is then the value for which the difference between trimmed V_{BE} and the ideal median value of V_{BE} is closest to zero. This can be evaluated with the *cross* calculator function which has two inputs – an examined signal and a threshold. The function outputs the X-value for which the value of the examined signal is equal to the threshold. If the X-axis variable is the trimming code and the examined signal is the difference between the trimmed and ideal V_{BE}, this function returns the correct trimming code.

The code then needs to be passed from one simulation test to another. This can be done using the `calcVal` function. This function cannot be used in the calculator but instead it accesses the results database. The syntax is `calcVal("expression_name" "test_name")` where `expression_name` is the name of the expression whose value should be transfered and `test_name` is the name of the simulation test which evaluates said expression. It should be used in the *Design Variables* section of the `trimmed` test – not the *Global Variables* section as that is common to all tests.

The second test `trimmed` can therefore easily access the trimming code and use it to sweep temperature and evaluate the temperature reading error at various points of the range. Second problem arises, however, when the trimming code has to be determined using transient analysis, which is the case when DEM and chopping are implemented. This is because the trimmed V_{BE} itself has to be evaluated using averaged transient signals (averaging the transient signals is basically performing the role of the DSP).

The solution is as follows. The difference between the trimmed and ideal V_{BE} at various trimming code values will be evaluated normally in transient analysis using the *average* function. However, instead of evaluating it in each point, it should be evaluated over corners – this is done by selecting *evalType* in the *Outputs* section

as `corner` instead of `point`. This is because the trimming code will be swept not parametrically but in individual corners, and the proper trimming code has to be evaluated across all the corners.

A potential advantage of the V_{BE} trim method is the fact that during the `untrimmed` test, the only DEM and chopping algorithms that have to be running are the ones in the biasing circuit. The DEM and chopping algorithms in the CTAT and PTAT generators can be turned off as the signal of interest is the trimmed V_{BE}, which significantly improves the simulation time. This is helpful because the simulation time is already more than considerable even with the PTAT and CTAT generator algorithms turned off. With Accelerated Parallel Simulator option and the unnecessary DEM cycles turned off, one run of the `untrimmed` test takes up about a minute. As the trimming circuit is 6-bit, precisely 64 transient simulations simulating one full chopping period (50 ms) have to be done for each Monte Carlo run to sweep all the possible codes, and several hundreds of these Monte Carlo runs have to be done to gain statistically significant results. Then, the evaluated trimming codes have to be transferred to the `trimmed` test, where all the DEM and chopping cycles have to be running to properly evaluate the precision of the sensor. Because this increases the amount of switching transients significantly, the simulation time increases to about five minutes for single transient run at a single temperature. Because the temperature dependence of the error is of interest, about 8 temperature points (−55, −25, 0, 25, 50, 75, 100 and 125 °C) are required for each Monte Carlo run, of which there are hundreds. In total, full trimming simulation of 200 chips can take up to few days. Parallelization and distributed computing is necessary to reduce the simulation time to reasonable amount.

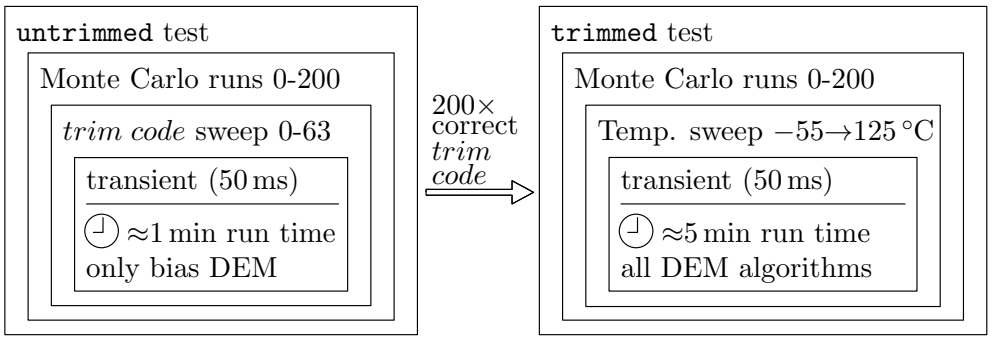

Fig. A.1: Trimming simulation overview

If the output trim method were to be simulated, all the DEM and chopping algorithms would have to be running even in the `untrimmed` test. This would increase the overall simulation time significantly, which is why this method has not been tried even though it might lead to better results.

B FEEDBACK LOOP STABILITY ANALYSIS

Two most extreme corner cases for the loop gain (solid lines) and phase (dashed lines) curves are shown to prove the unconditional stability of the feedback loops.

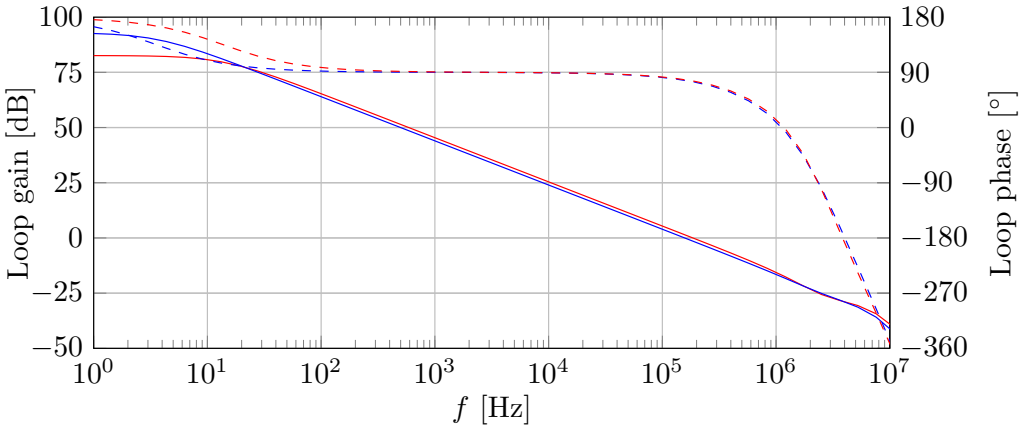

Fig. B.1: Biasing circuit feedback loop stability analysis

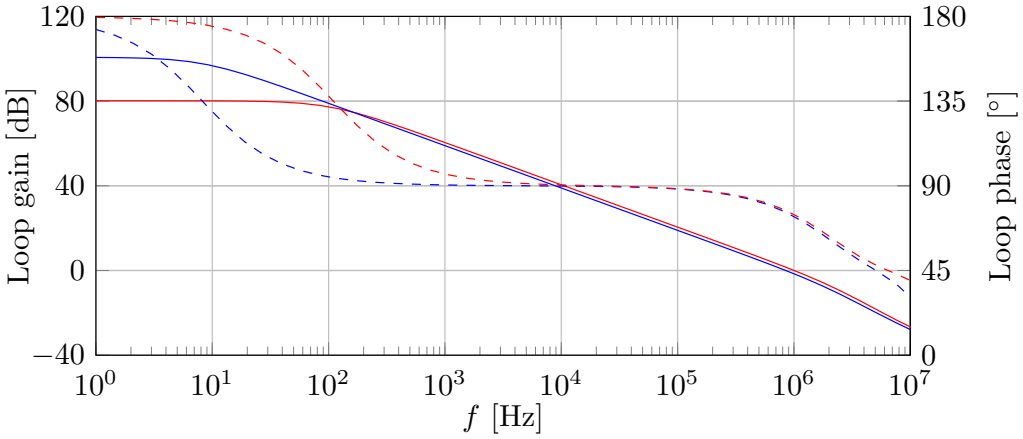

Fig. B.2: CTAT generator feedback loop stability analysis

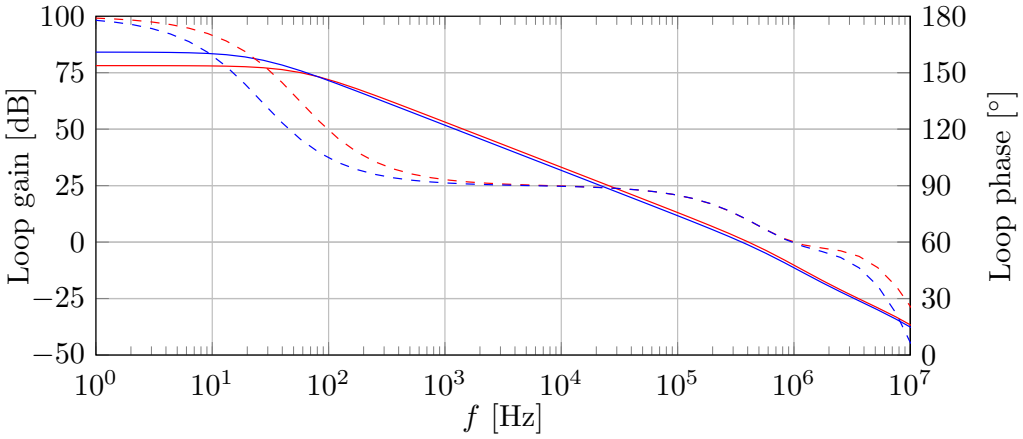

Fig. B.3: PTAT generator feedback loop stability analysis

C TEMPERATURE SENSOR ANALOG FRONT-END CADENCE SCHEMATICS

C.1 Top-level schematic

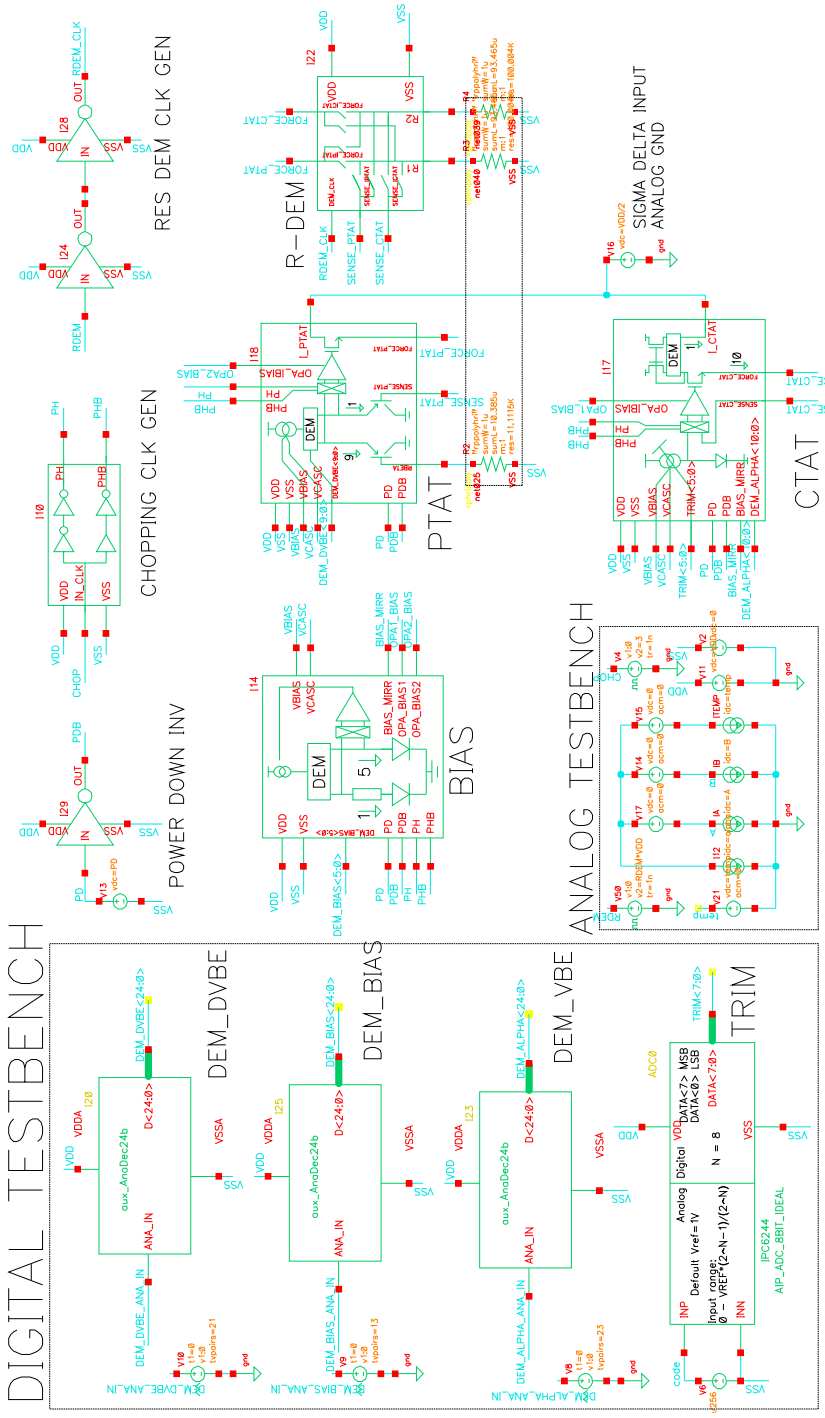

Fig. C.1: Top-level analog front-end schematic including testbench

C.2 Biasing circuit

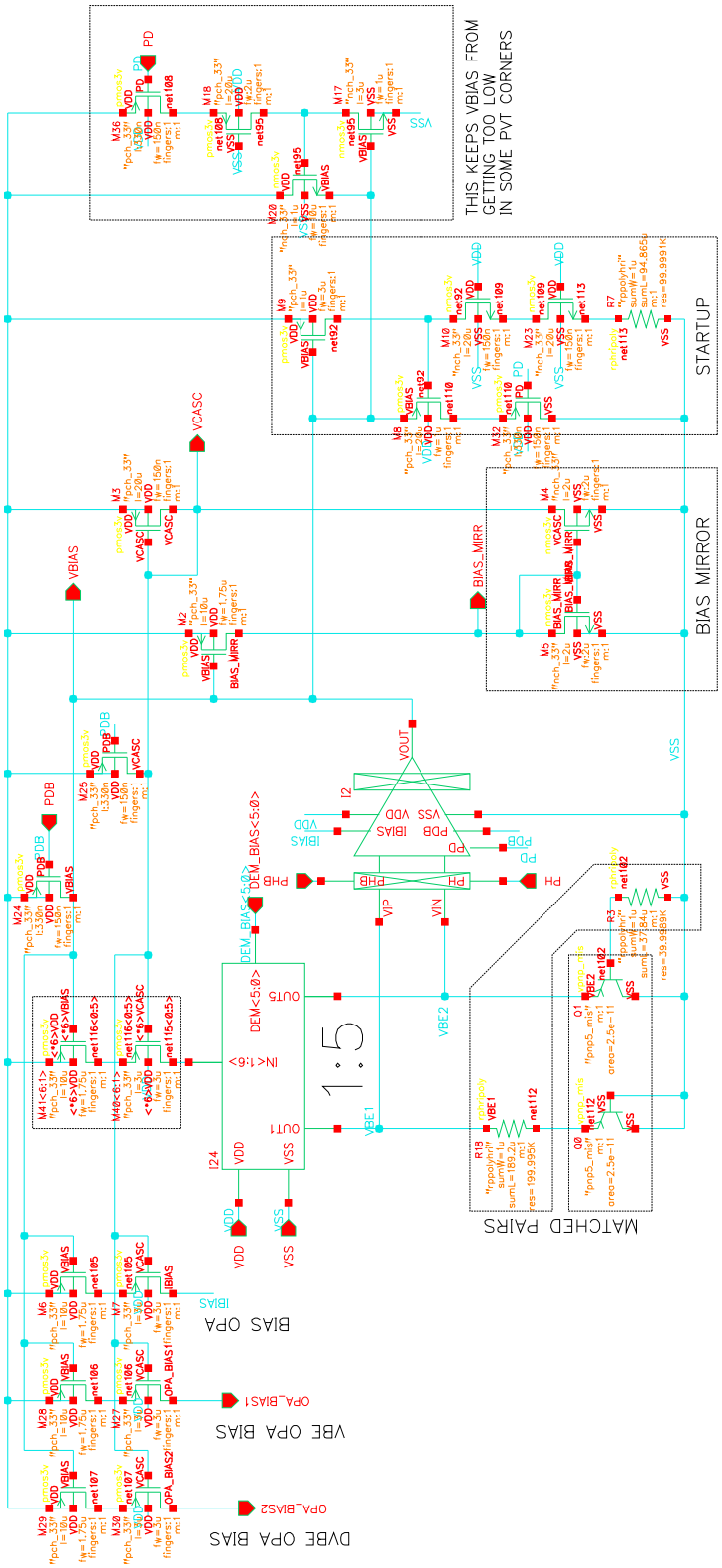

Fig. C.2: Biasing circuit schematic

C.3 CTAT generator

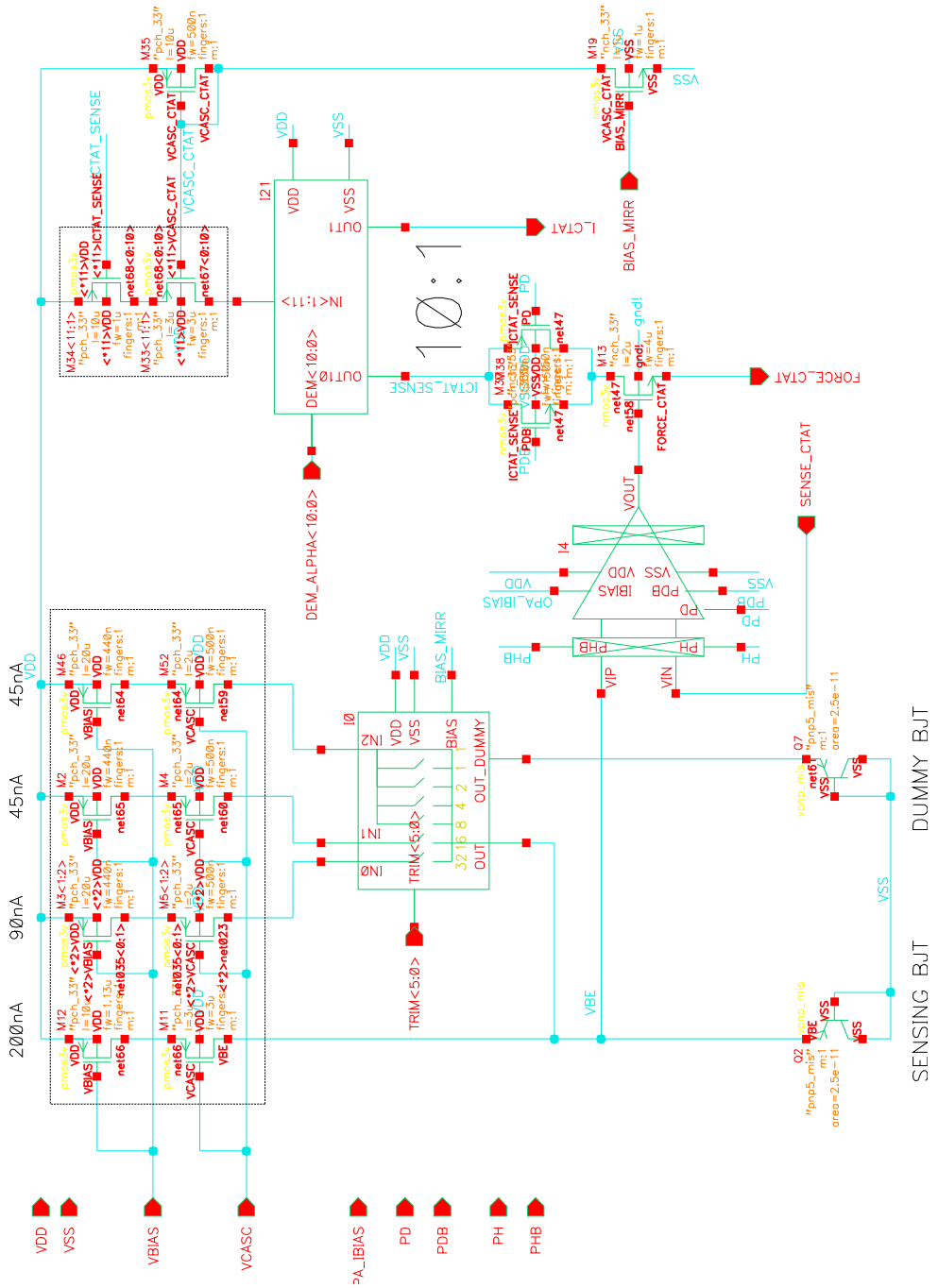

Fig. C.3: CTAT generator schematic

C.4 Resistor DEM controller

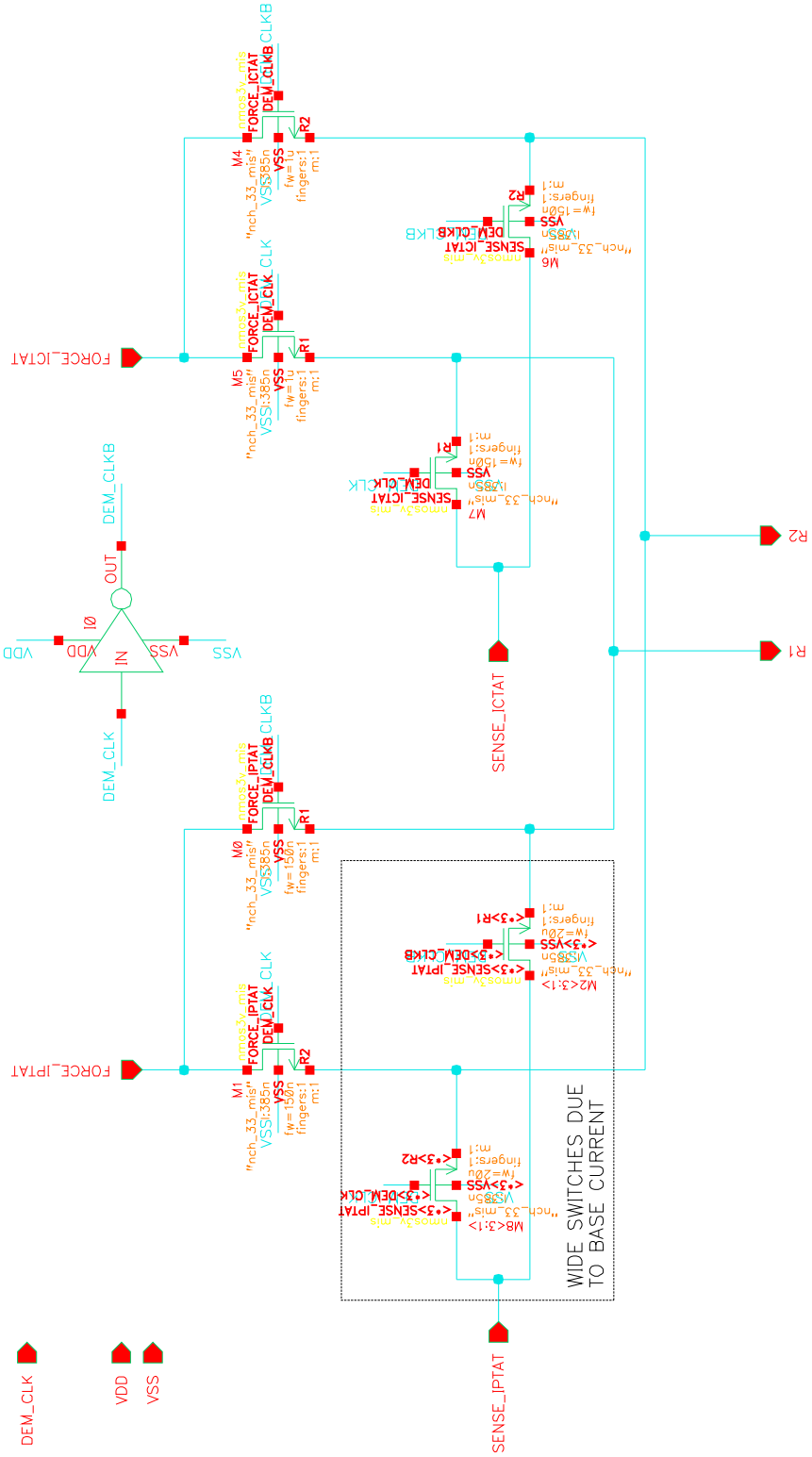

Fig. C.4: Resistor DEM controller schematic

C.5 Clock inverter circuit

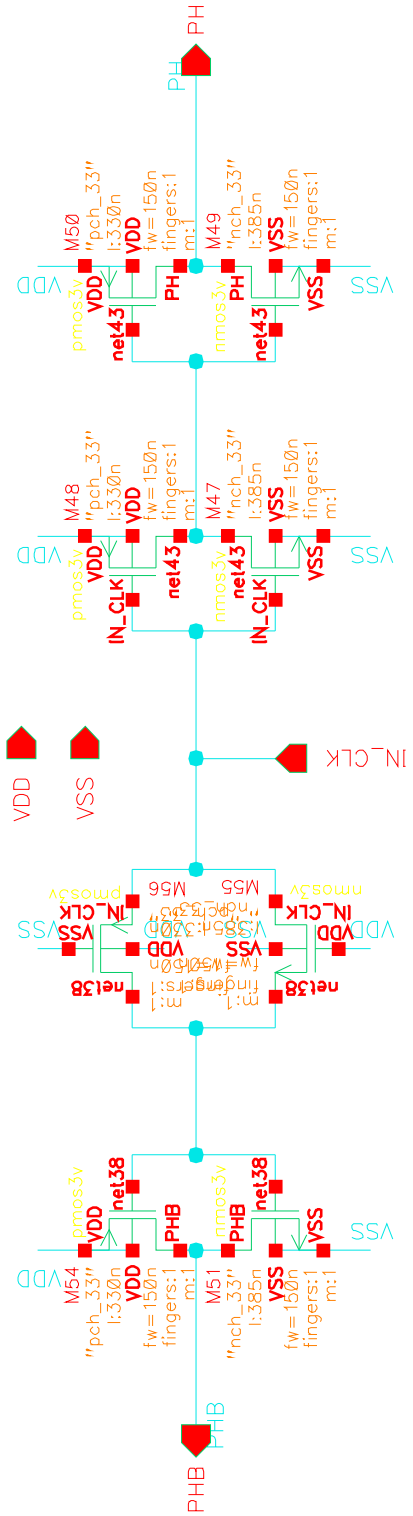

Fig. C.5: Clock inverter circuit schematic

C.6 PTAT generator

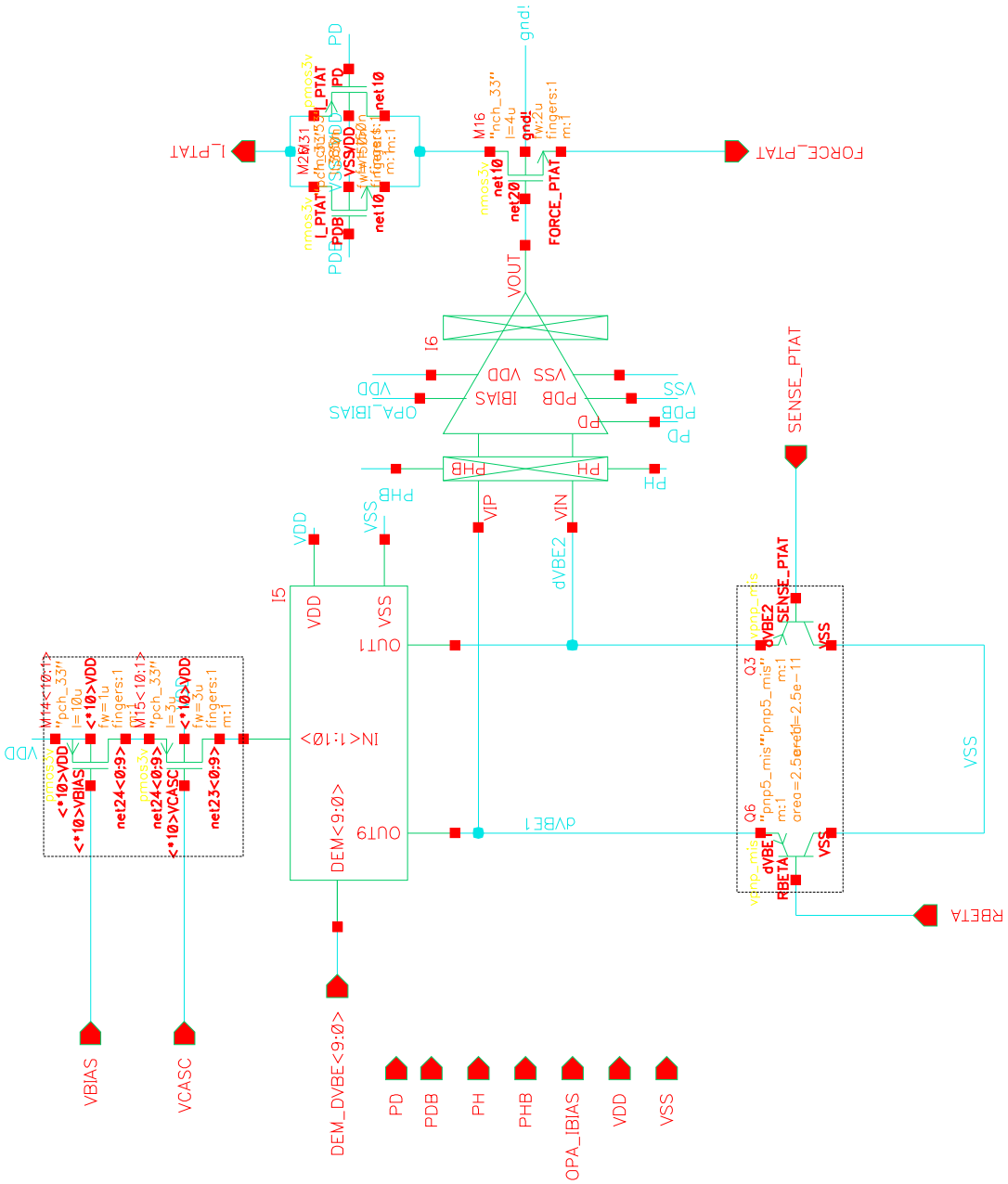

Fig. C.6: PTAT generator schematic

C.7 Trimming circuit

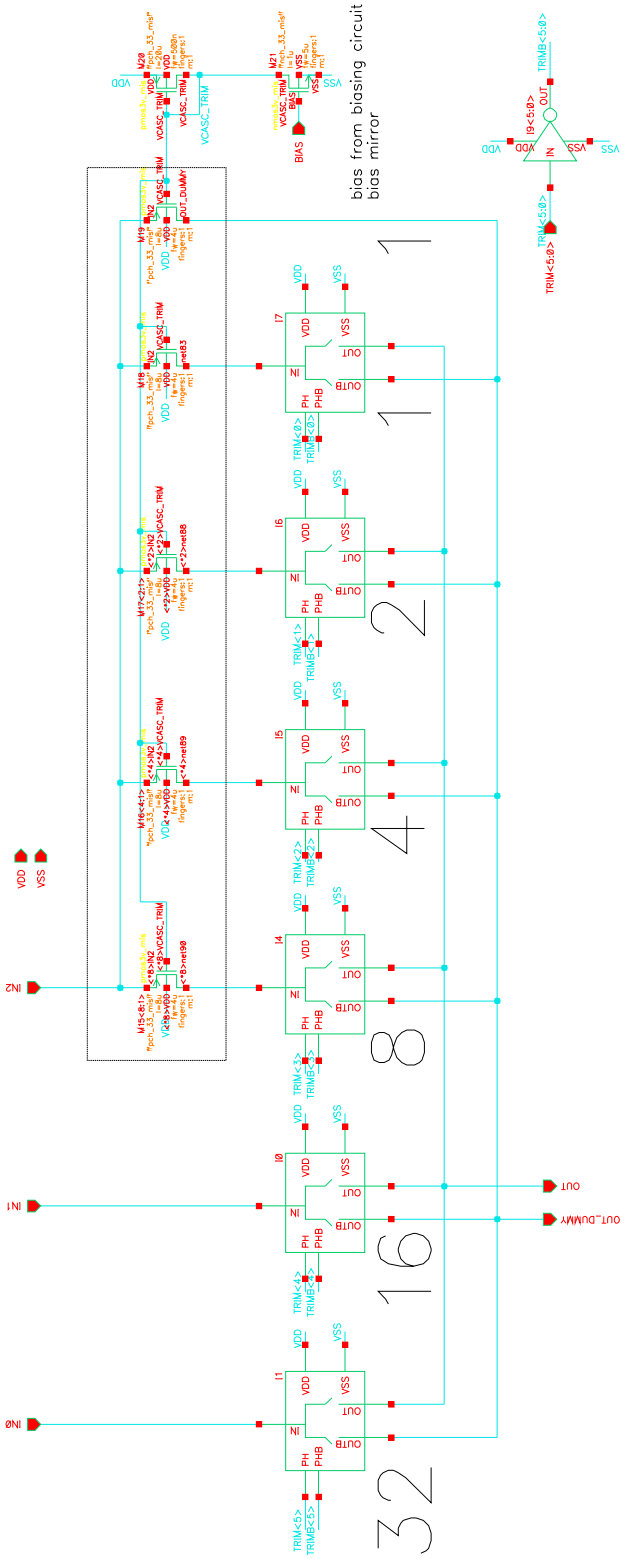

Fig. C.7: Trimming circuit schematic

C.8 PTAT mirror DEM controller

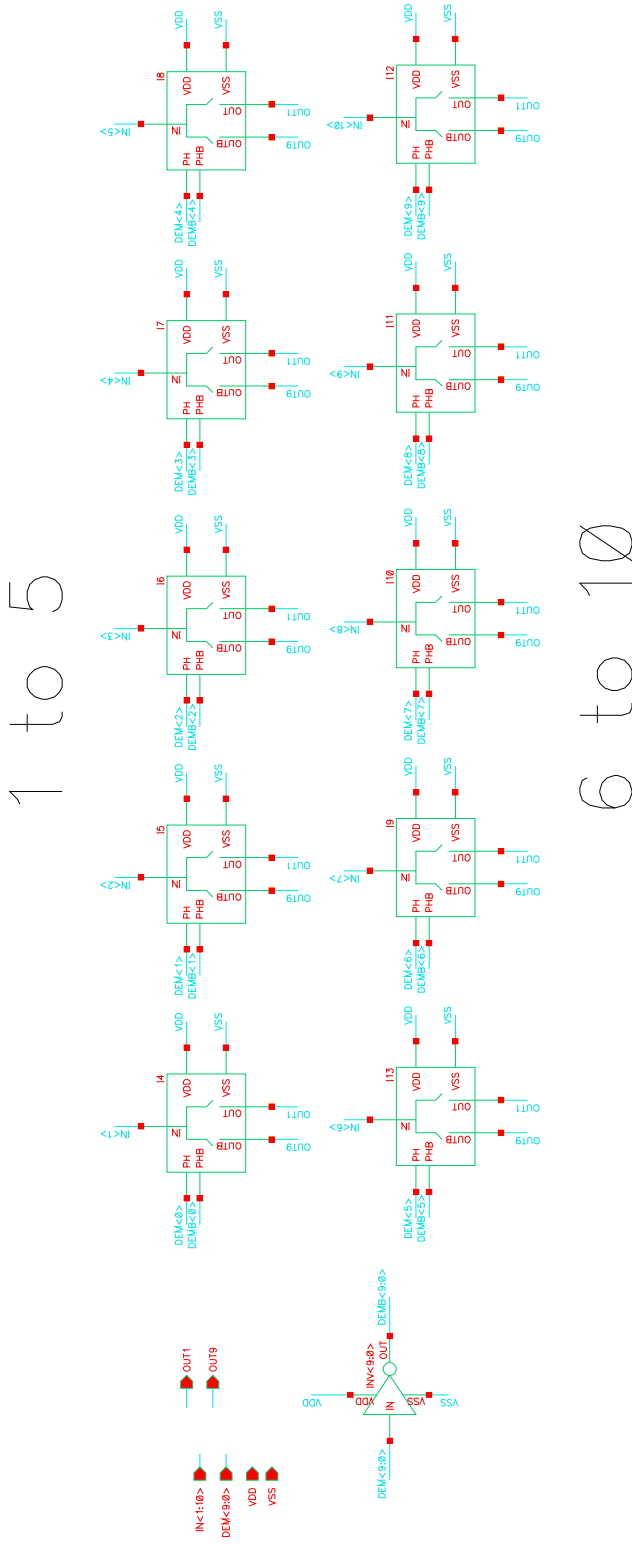

Fig. C.8: PTAT mirror DEM controller schematic

C.9 α-mirror DEM controller

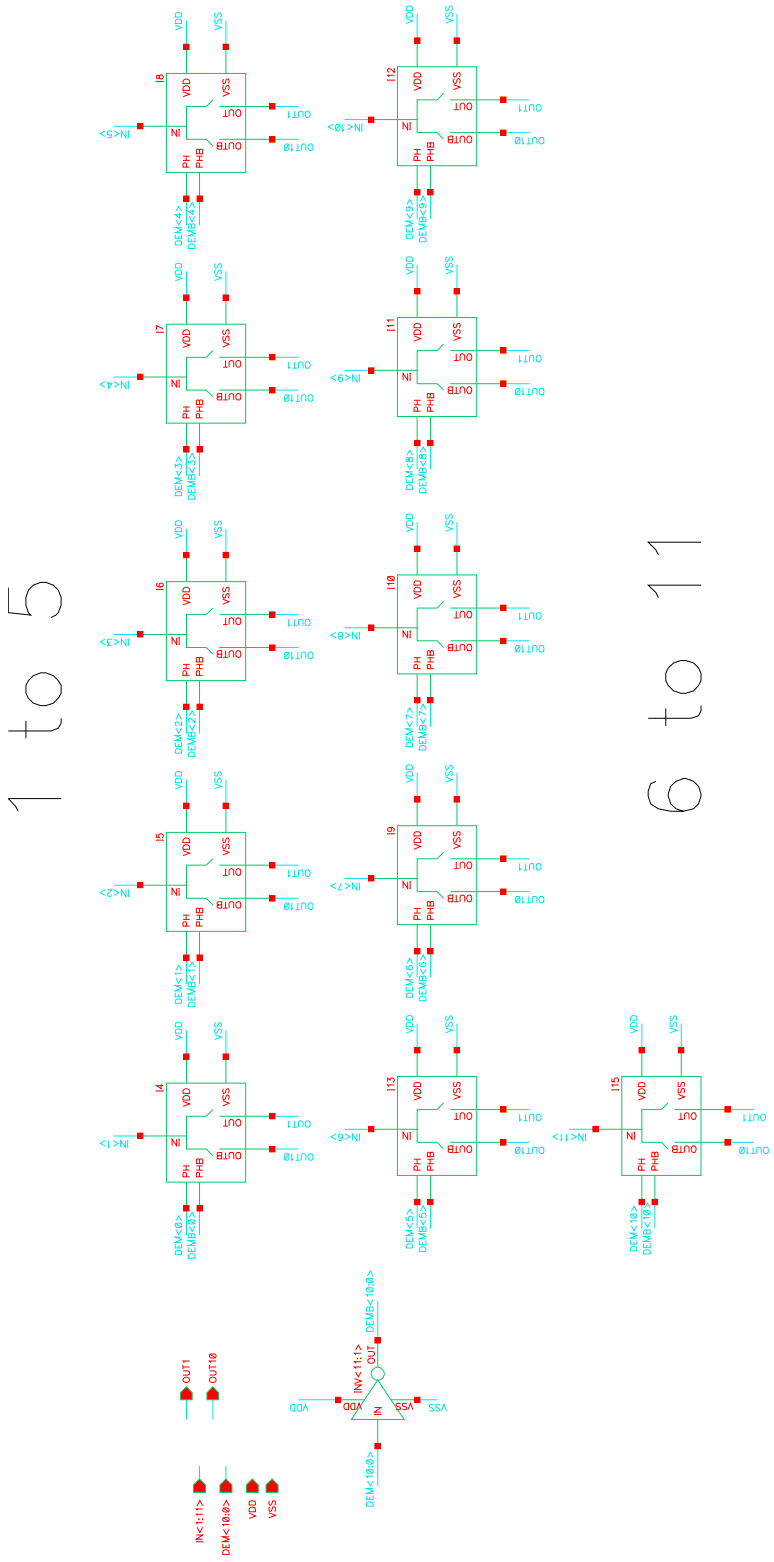

Fig. C.9: α-mirror DEM controller schematic

C.10 Biasing circuit mirror DEM control

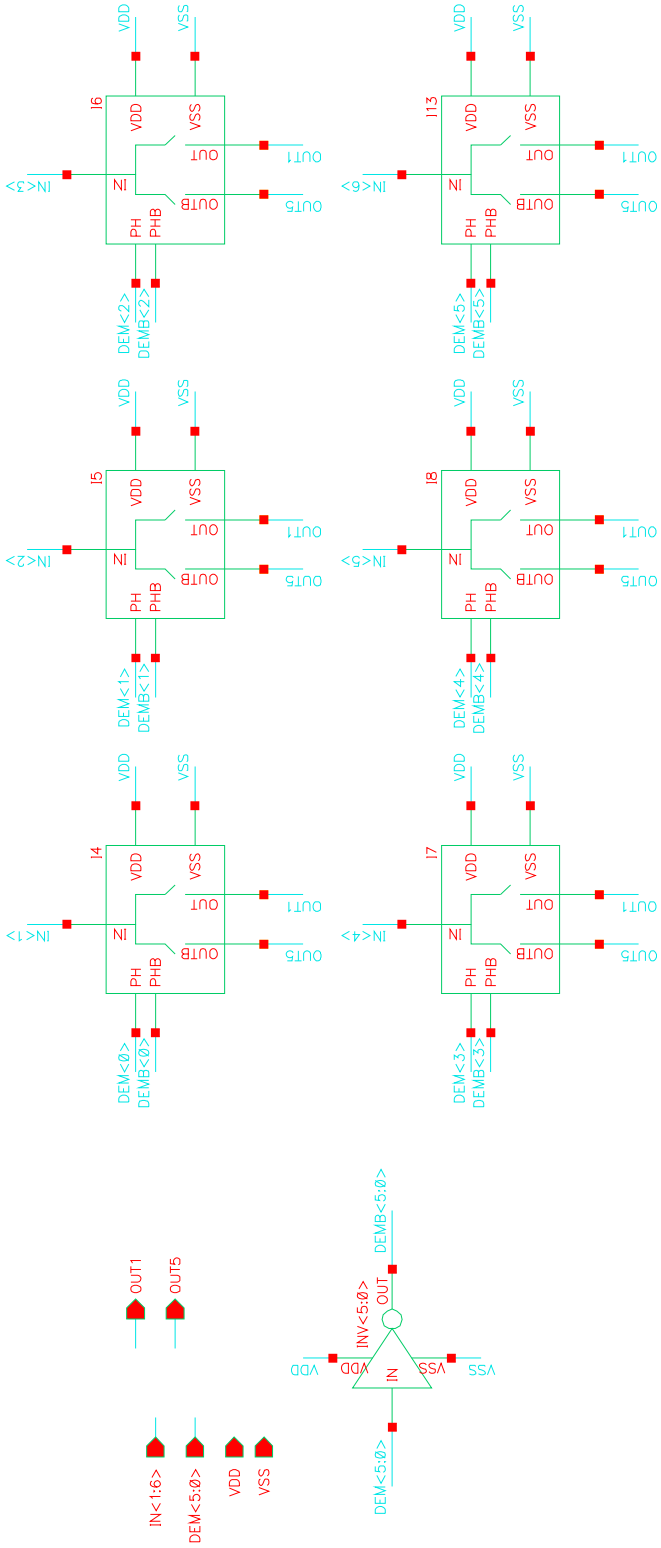

Fig. C.10: Biasing circuit mirror DEM control schematic

C.11 Biasing circuit and CTAT generator folded cascode chopped opamp

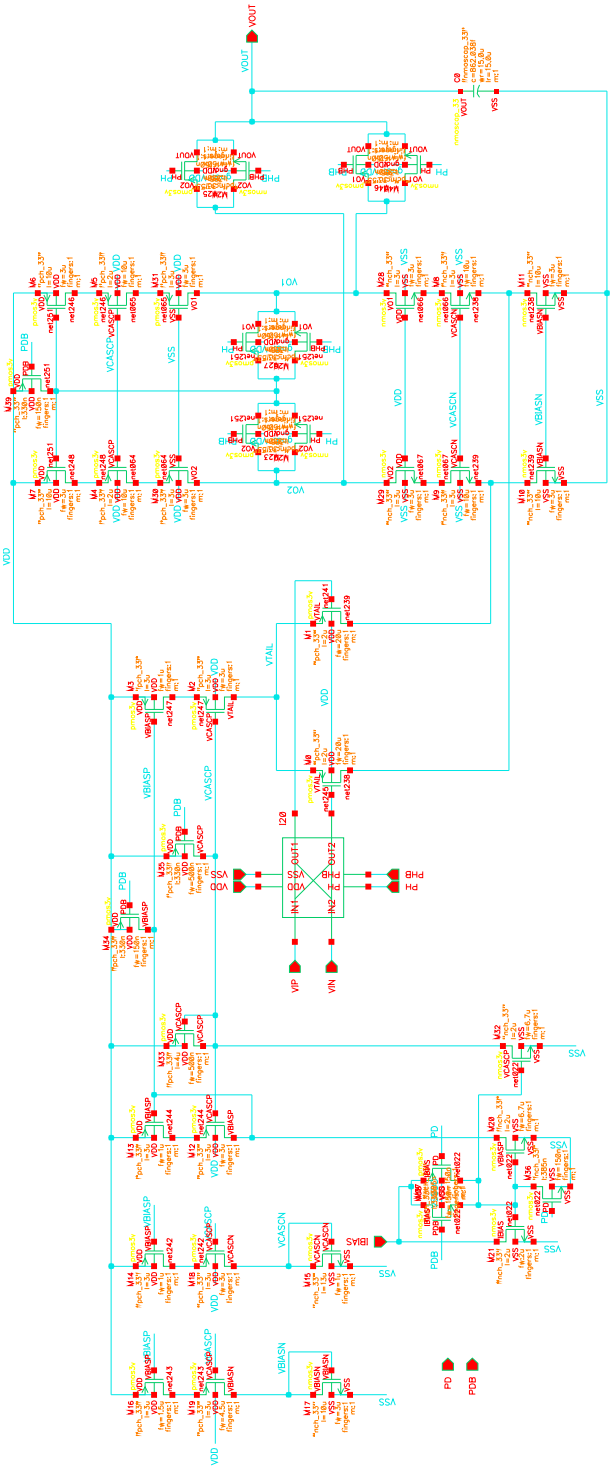

Fig. C.11: Biasing circuit and CTAT generator opamp schematic

C.12 PTAT generator folded cascode chopped opamp

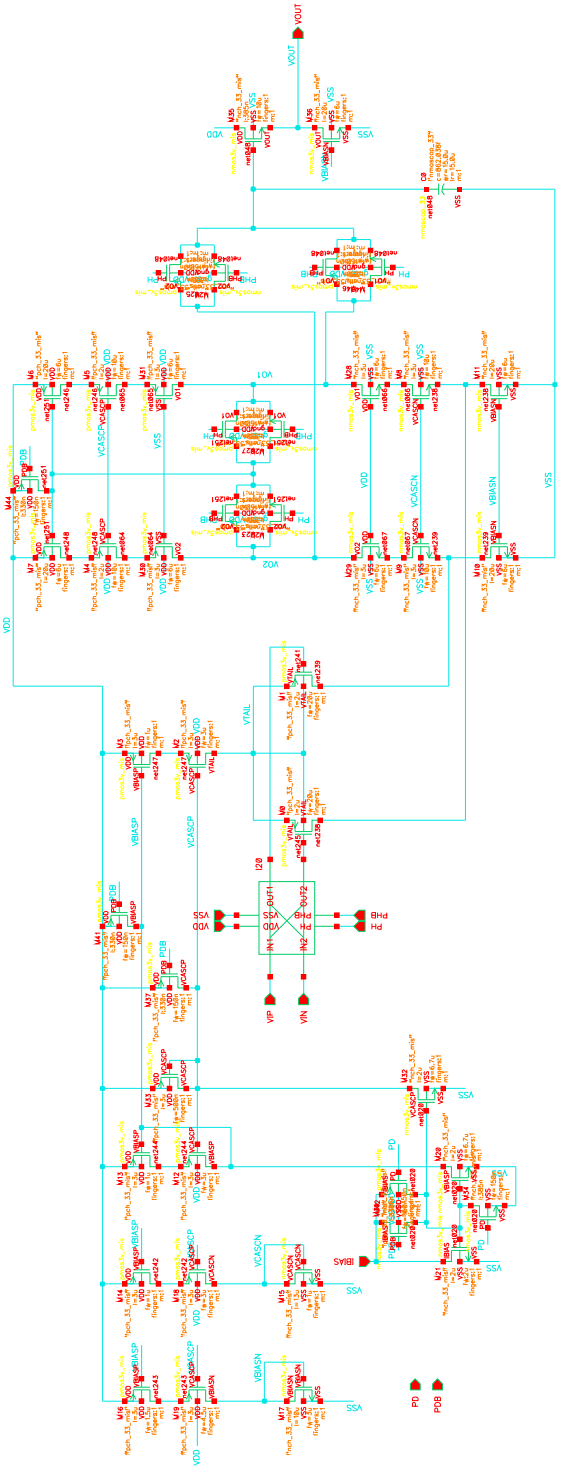

Fig. C.12: PTAT generator opamp schematic

C.13 Input chopping switch

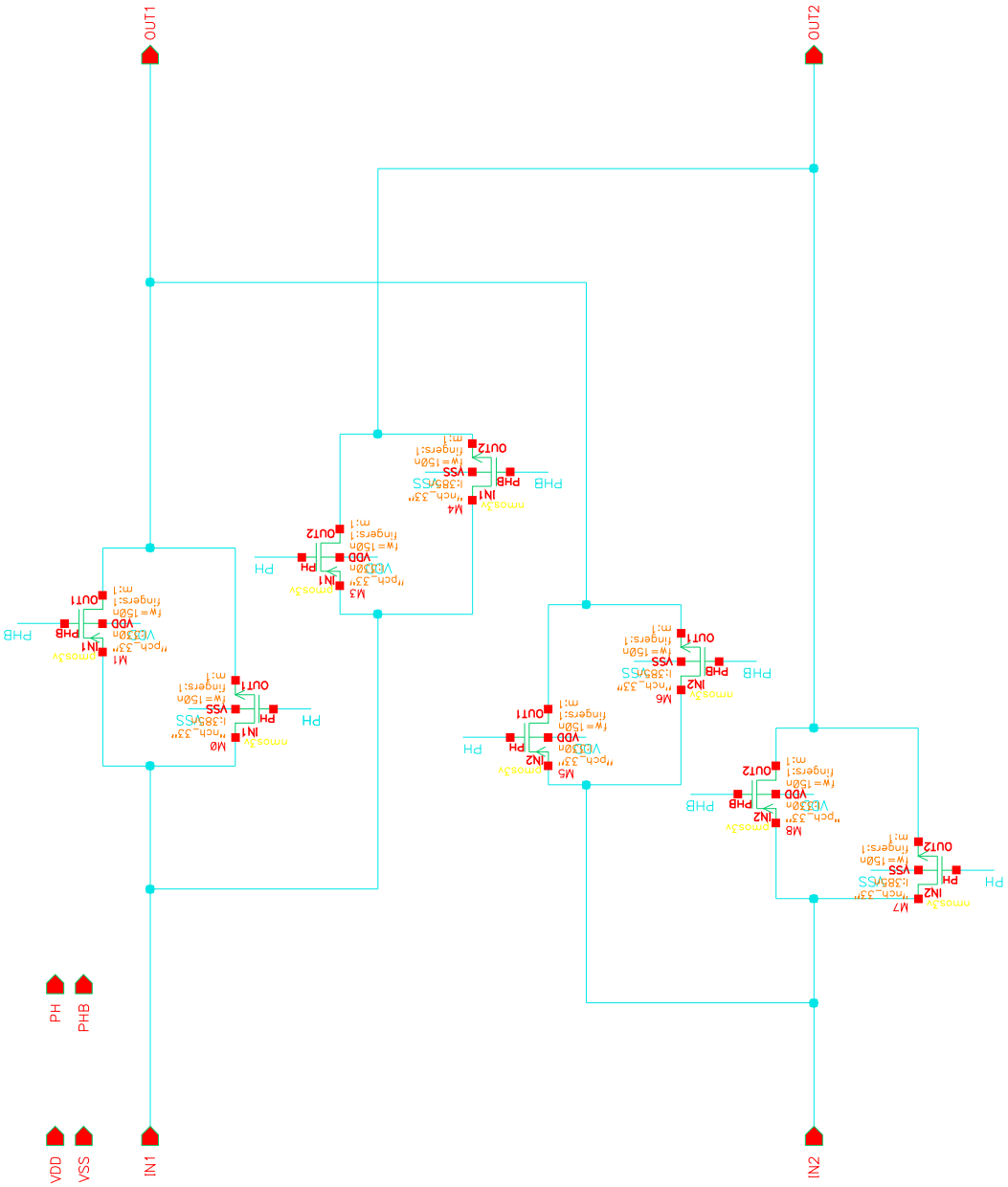

Fig. C.13: Input chopping switch schematic

C.14 DEM switch

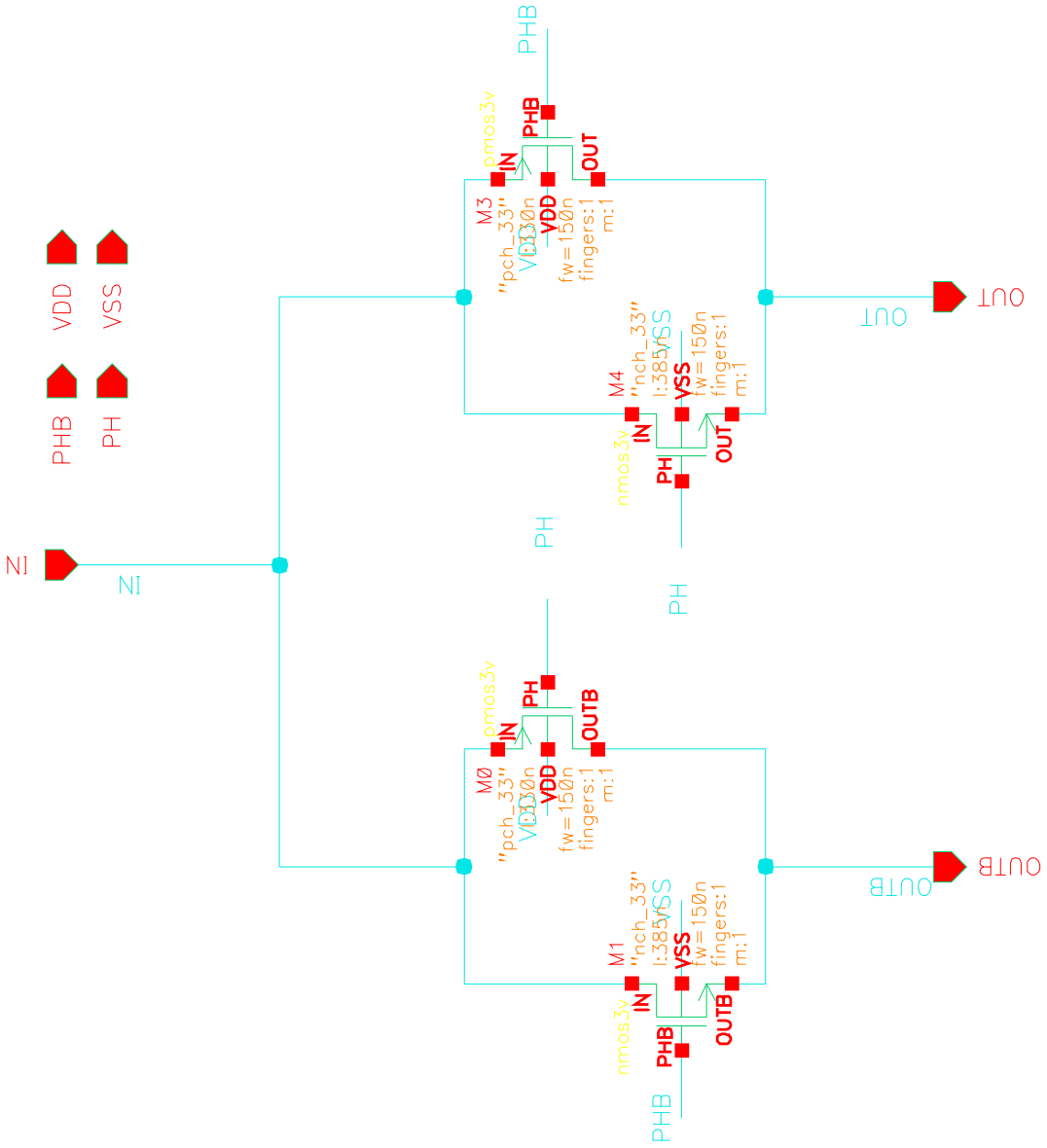

Fig. C.14: DEM switch schematic

C.15 Inverter gate

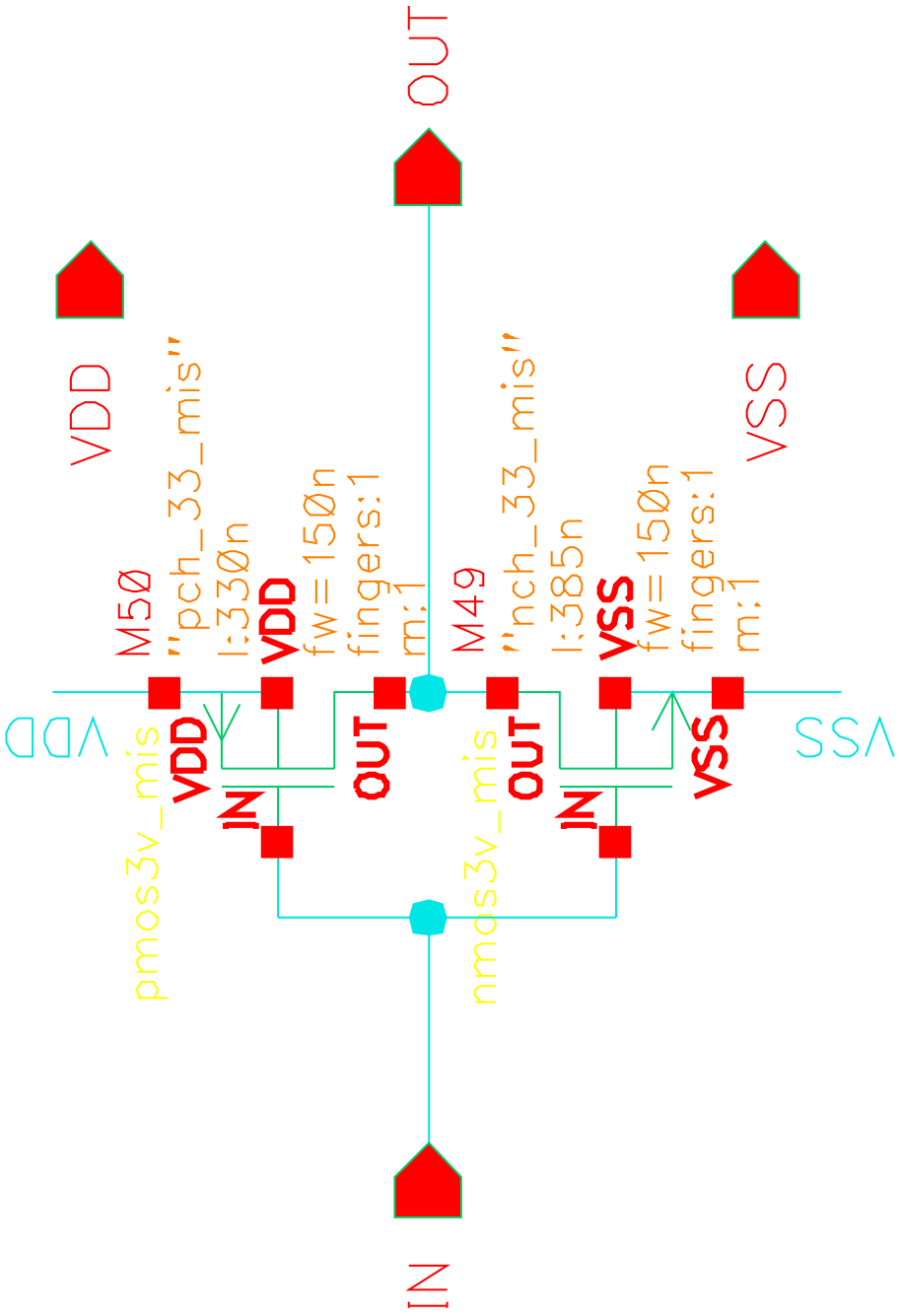

Fig. C.15: Inverter gate schematic